Mansoura University		Department: Computers Engineering And Systems Total Marks: 100 Marks	Faculty of Engineering

Course Title: دوائر رقمية ونبضية	Course Code: **6715**	**Final exam**
Date: Sep..8. 2013	Allowed time: 3 hrs	Master in automatic control

Remarks: *Attempt the following problems*

Q1- A Relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

a) What should be the value of the relative address field of the instruction (in decimal)?

b) Determine the relative address value in binary using 12 bits.(Why must the number be in 2's complement?)

c) Determine the binary value in PC after the fetch phase and calculate the binary value of 500. Then show that the binary value in PC plus the relative address calculated in part (b) is equal to the binary value of 500.

Q2)

a. Formulate two five-segment instruction pipelines for a computer. For each, specify the operations to be performed in each segment. Which one is more efficient? Why ?

b. Explain four possible schemas that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction hazards in CISC computers.

c. Show the block diagram of the BCD adder.

d. Using combinational circuit design techniques, derive the Boolean functions for the BCD 9's complementer. Draw the logic diagram.

Q3- What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?

a. How many characters per second can be transmitted over a 1200-baud line in each of the following modes? (Assume a character code of eight bits).
- Synchronous serial transmission.
- Asynchronous serial transmission with two stop bits.
- Asynchronous serial transmission with one stop bit.

Q4- Draw an algorithm in flowchart form for adding or subtracting two Floating Point numbers.

Q5- A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8 .The computer system needs 4K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, 10 for interface registers.

e. How many RAM and ROM chips are needed?

f. Draw a memory-address map for the system.

g. Give the address range in hexadecimal for RAM, ROM, and interface.

Q6- Obtain the Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive.

GOOD LUCK

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