An 8-Bit Full-Adder Implementation Using Single Electron Tunneling (SET) Technology

تنفيذ دائرة جمع_ كامل ذات ثمانية بت
بإستخدام تكنولوجيا إختراق الإلكترون الواحد (النانومترية)

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الخلاصة:

إن تكنولوجيا إختراق الإلكترون الواحد (النانومترية) تقدم إمكانية أكبر لتصغير أبعاد المكونات الإلكترونية الحديثة مقارنة بالإمكانيات المتوقعة لتكنولوجيات السيليكون المعروفة (مثل تكنولوجيا معدن_أكسيد_شبه موصل المزدوجة). إن تكنولوجيا إختراق الإلكترون الواحد تعطى القدرة على التحكم فى حركة الإلكترونيات فى الدوائر المصممة. فى هذا البحث سنقوم بإستعراض أحد دوائر الإلكترون الواحد فى الأبحاث المنشورة حديثا وهى الدائرة المنطقية الحدية (Threshold Logic Gate) وكيفية إستخدامها فى تنفيذ دائرة جمع ـ كامل ذات بت واحدة. وسيتضمن ذلك تفاصيل هذه الدائرة بما فيها قيم المكونات المستخدمة والنتائج المتوقعة لإستخدام هذه الدائرة بالاستعانة ببرنامج المحاكاه على الكمبيوتر (سيمون 2). ثم سنناقش إمكانية تكبير الدائرة السابقة لتنفيذ دوائر جمع ـ كامل ذات أعداد بت أكبر. وفى نهاية البحث سنقدم التصميم الكامل لدائرة إلكترون واحد تنفذ دائرة جمع ـ كامل ذات ثمانية بت مع نتائج المحاكاه على الكمبيوتر.

Abstract: Single Electron Tunneling (SET) devices have come to be considered as promising candidates for future ultra-low power and high-density integrated circuits. Their potential for ultra-low power is related to that the operation is based on only few electrons. The term Single Electron Tunneling (SET) technology has been selected for devices sensitive to the manipulation of a single electron even if the device itself requires in fact few electrons. Besides, SET provides simple and elegant solution for implementing Threshold Logic Gates (TLGs).

This paper presents a SET TLG one-bit full-adder implemented in SET technology. The paper then introduces the design and implementation of an 8-bit SET TLG full-adder and presents its SIMON 2 simulation results.

1 Introduction

Semiconductor Industry Association's (SIA's) 2003 International Technology Roadmap for Semiconductors (ITRS) introduced new technologies that may extend MOSFETs to the 22nm node (9nm physical gate length) by 2016 [1]. The 10nm gate length is labeled the CMOS showstopper region, where fundamental limitations are reached and new phenomena have to be dealt with [2]. It is generally accepted than sooner or later other emerging nanotechnologies will share CMOS in modern semiconductor industry. These new devices take advantage of the quantum mechanical phenomena that emerge at nanometer scale geometrics [2]. One of these promising technologies is the Single Electron Tunneling (SET) technology.

The SET technology is distinguished by a very small device size and ultra-low power dissipation. These two properties promise to allow large density integration without exceeding the power density physical limits [2]. While promising for helping to solve the power consumption challenge, SET is expected to be sensitive to variations and to background charge [3]. Such problems might be tackled by using fault-tolerant designs; while the low gain of SET devices suggest that they should be combined with CMOS [4].

An electron can tunnel through an insulator if the distance between the conductors is small enough. A metal-insulator-metal structure is called a single-electron tunneling junction. Due to this layout a SET junction can be modeled as a capacitor, when no tunnel events occur. SET circuits are centered on the SET tunnel junction, through which individual electrons can be transported in a controlled matter. Also, SET provides simple and elegant solution for implementing linear Threshold Logic Gates (TLGs) [4]. Our research focuses on the implementation of logic functions in SET technology using TLGs. One of these

logic circuits is the full adder circuit. The remainder of this paper is organized as follows: Section 2 briefly presents the background material about the TLG and the static buffer. Section 3 describes full adder threshold implementation. Single-electron threshold logic full-adder is described in Section 4. Section 5 presents multi-bit threshold full-adder and the SIMON 2 simulation results of an 8-bit SET TLG full-adder.

2 The Threshold Logic Gate and The Static Buffer

The Threshold Logic Gate (TLG) is the simplest artificial neuron which computes the sign of the weighted sum of its inputs and compares this sum with a threshold value. If the sum is larger than the threshold, the TLG outputs a one, otherwise the output will be zero. Mathematically, a TLG implements a function,

$$f(x_1,..., x_\Delta) = sign\left(\sum_{j=1}^{\Delta} w_j x_j - \theta\right), \quad (1)$$

where w_j is the weight associated with x_j, θ is the threshold, and Δ is the fan-in [6].

A majority gate (MAJ) is a special TLG having unity weights ($w_1 = w_2 = ... = w_\Delta = 1$) and a threshold equals to half the number of weights ($\theta = \Delta/2$, where $\Delta=2k+1$: k is any integer ≥ 1).

$$MAJ(x_1,..., x_\Delta) = sign\left(\sum_{j=1}^{\Delta} w_j x_j - \Delta/2\right), \quad (2)$$

In practice, the integer threshold θ is reduced by 0.5 to improve on the noise margins. Also, TLG will be represented by the series of its weights and practical threshold ($w_1.... w_\Delta$; $\theta - 0.5$), while a MAJ gate is represented by (1, 1, ..., 1; $\Delta/2-0.5$) [4].

TLG can be used as a basis for implementing Boolean logic gate [5]. The individual gates operate correctly in simulations but strong feedback effects

occur in networks of these gates, due to this behavior the buffer is required in order to reduce the sensitivity of these gates to the feedback effects which occur in a network.

The static inverting buffer consists of two SET transistors attached to a single load capacitor as shown in figure 1. The circuit operates as follows. If the input $V_i = 0$ and the total charge on node n2 is 0, the upper SET transistor removes 1 electron from the output node n2 , resulting in the output $V_o = '1'$. If the input $V_i = '1'$ and an electron has been removed from the output node n2, the lower SET transistor adds one electron to node n2, resulting in the output $V_o = '0'$.
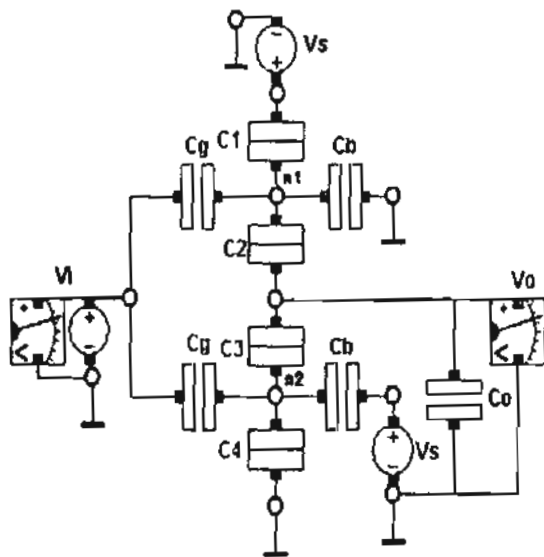

Fig. 1. SIMON 2 schematic for the static inverting buffer.

3 The Full-Adder Threshold Logic Implementation

The Full Adder (FA) is a basic arithmetic block which has three inputs: the addend A (1-b precision), the augend B (1-b precision), and the carry-in C_i; and two outputs: the sum S and the carry-out C_o. An established method for computing S and C_o is

$$S = (A \oplus B \oplus C_i) \ (3)$$

$$C_o = (A \wedge B) \vee (A \wedge C_i) \vee (B \wedge C_i) \ (4)$$

where we have used the following notation: $\wedge$ for logic AND, $\vee$ for logic OR, and $\oplus$ for logic XOR, while x * will represent the complement of a signal x.

To implement adders using TLGs, the sum and carry functions should be linearly separable. The carry does satisfy this condition, and be written as

$$C_o = sign(A + B + C_i - 1.5) \ (5)$$

which is a MAJ function. On the other hand, the sum function as expressed in (3) is not linearly separable. However, it can be represented in a linearly separable from by writing it in terms of both the carry-in (C_i) and carry –out (C_o).

$$S = (A \wedge B \wedge C_i) \vee [C_o * \wedge (A \vee B \vee C_i)] \ (6)$$

which can be written as:

$$S = sign(A + B + C_i - 0.5) \ (7)$$

By simple and algebra, the negative weight can be made positive (by inverting the associated input and modifying the threshold [6]), hence the function can be written as

$$S = sign(- A * - B * - C_i * + 2C_o * - (-0.5)) \ (8)$$

A simple procedure to obtain the threshold equations (7) and (8) is as follows:

- Equation (6) is written in a simplified sum –of – product from :

$$S = (A \wedge B \wedge C_i) \vee (C_o * \wedge A) \vee (C_o * \wedge B)$$
$$\vee (C_o * \wedge C_i)$$

- If A, B, and C_i are assigned a weight of 1, C_o* should be assigned a weight of 2 to make all the product terms equivalent. This weight can be negative (using C_o) or positive (using C_o*). Hence the threshold equation becomes;
$$S = sign(A + B + C_i - 2C_o * - \theta1) \quad \text{or}$$
$$S = (- A * - B * - C_i * + 2C_o * - \theta2).$$

(See eq. (1) for the definition of a threshold function).

- To determinate the threshold θ_1 and θ_2, two weight maps in addition to the Karnaugh map are created. This is illustrated in Fig. 2.

  o In the K-map (Fig. 2(a)), don't care (Φ) symbols are assigned to all the impossible combinations of A, B, C_i, and C_o.

  o The weight map in Fig. 2(b) shows the weighted sum of inputs using a negative weight: $A + B + C_i - 2C_o$.

  o The weight map in Fig. 2(c) shows the weighted sum of inputs using a positive weight : $-A^* -B^* -C_i^* +2C_o^*$

- Comparing each of the two weight maps with the K-map, it is clear that:

  o In Fig. 2(b) logic 0 corresponds to 0 and logic 1 corresponds to 1, hence the threshold $\theta_1 = 0.5$.

  o In Fig. 2(c) logic 0 corresponds to -1 while logic 1 corresponds to 0, hence the threshold $\theta_2 = -0.5$.

4 1-bit Single Electron Threshold Full-Adder

Single-electron threshold FA was proposed by Lageweg et al, [6]. This FA consists of two TLGs with a buffer for each one of them (Fig.3 (a)). The sum function is implemented by a $(-1, -1, -1, 2, -0.5)$ TLG, and the carry is implemented by a MAJ. Figure 3 (b) shows the $(-1, -1, -1, 2, -0.5)$ TLG. It consists of one single-electron

junction and five input and bias capacitors. The input signals V_1, V_2, V3 are weighted by their corresponding capacitors C and subtracted from the voltage across the junction.

The input signals V_4 is weighted by $2C$ and added to the voltage across the junction (i.e. implementing a negative weight). The bias voltage V_b weighted by the capacitor C_b is based to adjust the threshold. This FA structure (including two static buffers) uses 10 tunneling junctions and 21 capacitors. The values used for simulations are $C_{bc} = C_{bs} = 11.25$ aF for both TLGs and $C_b = 4.23$ aF for both buffers. The other parameters are $C_n = 0.5$ aF, $C_{j1} = C_{j4} = 0.1$ aF, $C_{j2} = C_{j3} = 0.5$ aF, $C_0 = 9$ aF, $R_j = 100$ KΩ, $C_L = 9$ aF, $V_S = 16$ mV and an operating temperature $T = 0K$. SIMON [7] schematic for threshold FA is shown in Fig. 4. The input signals A, B, and C_i used in this simulation, is shown in Fig. 5 (a), where the voltage levels (0 mV and 16 mV). The S output is shown in Fig. 5 (b).

5 Design and Simulation of an 8-Bit Threshold Full-Adder

In this section, the design and simulation of the 1-bit Single-electron threshold FA (presented in section IV) are extended to multi-bit full-adder. On the design side, considering future large scale logic circuit, it is important to design them in a way that

C_iC_o	00	01	11	10
A B				
0 0	0	Φ	Φ	1
0 1	1	Φ	0	Φ
1 1	Φ	0	1	Φ
1 0	1	Φ	0	Φ

C_iC_o	00	01	11	10
A B				
0 0	0	-2	-1	1
0 1	1	-1	0	2
1 1	2	0	1	3
1 0	1	-1	0	2

C_iC_o	00	01	11	10
A B				
0 0	-1	-3	-2	0
0 1	0	-2	-1	1
1 1	1	-1	0	2
1 0	0	-2	-1	1
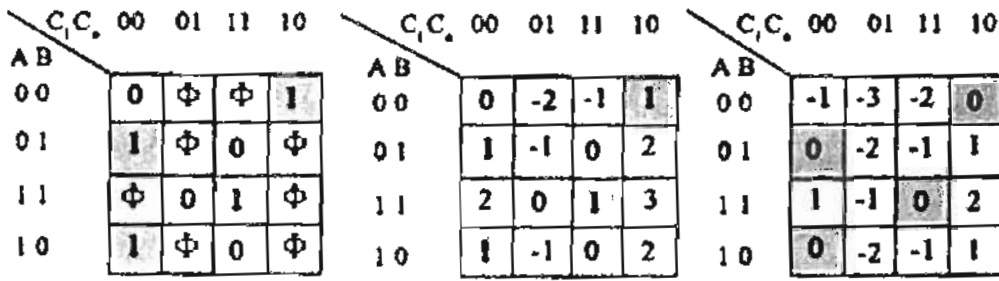
Figure 2. Mapping of a Boolean function to a threshold function (a) K-map of the Boolean function $S = (A \wedge B \wedge \wedge C_i) \vee (C_o{}^* \wedge a_j) \vee (C_o{}^* \wedge b_j) \vee (C_o{}^* \wedge C_i)$ (b) Weight map showing the sum of weights $A + B + C_i - 2C_o$. (c) Weight map showing the sum of weights $-A^* - B^* - C_i^* + 2C_o^*$.

(a)   (b)

Fig. 3. (a) Threshold logic Full Adder. (b) Threshold logic gate (TLG).

Fig. 4. SIMON schematic for Threshold logic FA.

Fig. 5. SIMON 2 Simulation results for the SET threshold full-adder.

Fig. 6. The Multi-bit full adder.

takes full advantage of SET. TLGs are good candidates for reducing the number of SET elements of the circuit, hence they are considered for this adder design. On the simulation side, this section presents the simulation results for 8-bit threshold adder. Multi-bit adder can be constructed by combining full adders in a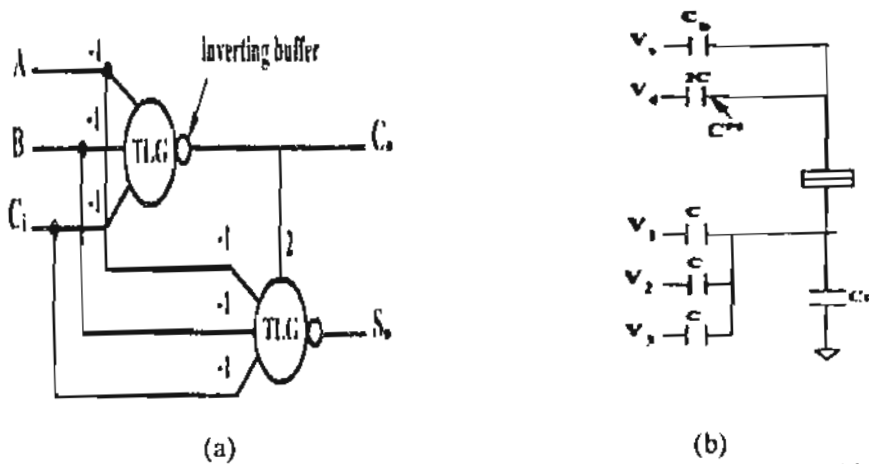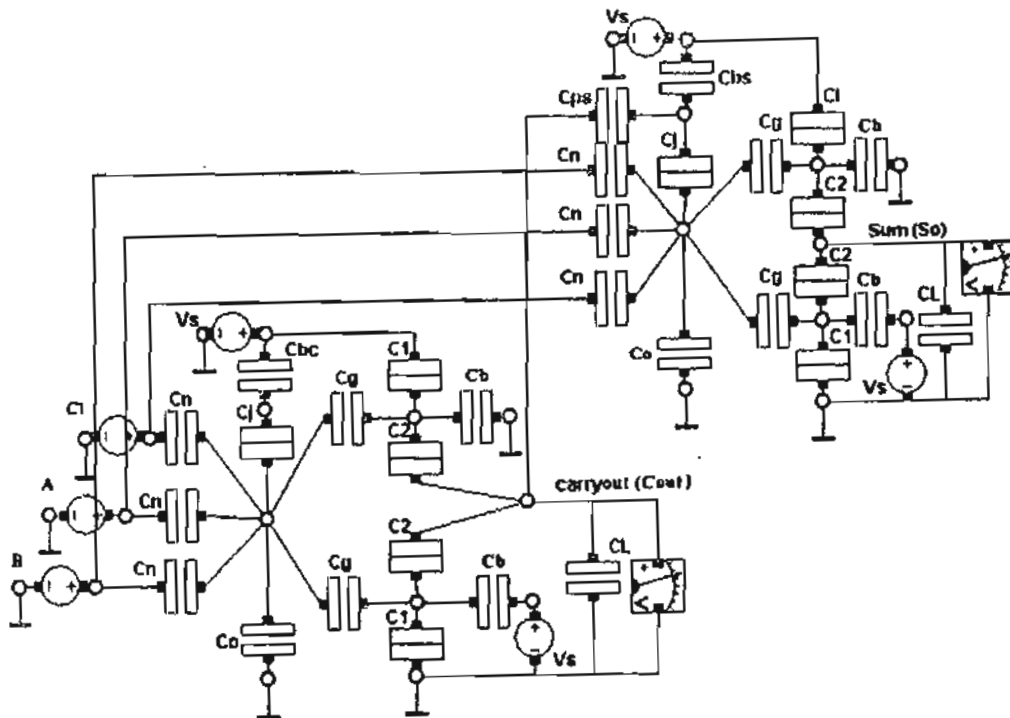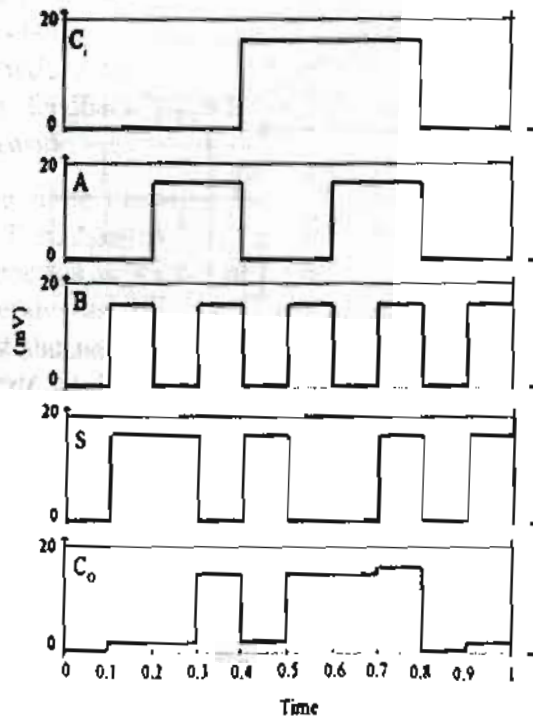 cascade configuration (by chaining the carry out of one full adder into the carry in of the full adder for the next bit) as shown in Fig. 6. Each full-adder block in Fig. 6, is the Threshold logic FA shown in Fig. 4.

The circuit parameters used in this simulation are the same parameters used in section IV, except the value of the positive weight capacitor for sum gate (C^{ps}), any

value in the range $2C < C^{ps} < 3C$ can be used in the design, hence $C^{ps} = 1.2$ aF was used in this design, where $C = 0.5$ aF. The SIMON 2 simulation results for the 8-bit full-adder are displayed in Fig. 7. All the simulation results are shown in Table I, which provides the carry out results of each stage.

5 Conclusions

In this paper, the background material about the TLG and the static buffer (added to overcome feedback effects which appear in SET networks) was presented. A 1-bit TLG FA was presented using SET technology. This FA consists of two TLGs with a static buffer added after each TLG. Finally, the design and SIMON 2 simulation results of an 8-bit SET TLG FA were introduced.

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Fig. 7. SIMON 2 Simulation results for

the 8-bit SET threshold full-adder.

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TABLE 1

Truth Table of Simulation Results for the 8- bit Threshold Full-Adder

C_0	A	B	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1