AN 8-BIT DAC IMPLEMENTATION USING SINGLE ELECTRON TUNNELING (SET) TECHNOLOGY

تنفيذ دائرة محول-رقمى-تماثلى ثمانية بت باستخدام تكنولوجيا إختراق الإلكترون الواحد (النانومترية)

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الخلاصة:
إن تكنولوجيا إختراق الإلكترون الواحد (النانومترية) تقدم إمكانية أكبر لتصغيرأبعاد المكونات الإلكترونية الحديثة مقارنة بالإمكانيات المتوقعة لتكنولوجيات السيليكون المعروفة (مثل تكنولوجيا معدن-أكسيد-شبه موصل المزدوجة). إن تكنولوجيا إختراق الإلكترون الواحد تعطى القدرة على التحكم فى حركة الإلكترونيات فى الدوائر المصممة. فى هذا البحث سنقوم بإستعراض أحد دوائر الإلكترون الواحد الأساسية فى الأبحاث المنشورة حديثا وهى دائرة تحريك الشحنات وكيفية إستخدامها فى تنفيذ دائرة محول-رقمى-تماثلى أربعة بت. وسيتضمن ذلك تفاصيل هذه الدوائر بما فيها قيم المكونات المستخدمة والنتائج المتوقعة لإستخدام هذه الدوائر بإستخدام برنامج المحاكاه على الكمبيوتر (سيمون 2). ثم سنناقش إمكانية تكبير الدائرة السابقة لتنفيذ محولات ذات أعداد بت أكبر وسنجد أن الحد الأقصى الذى يمكن الوصول إليه بإستخدام القيم المقترحة للدائرة المذكورة هو محول ستة بت. وفى نهاية البحث سنقدم التصميم الكامل لدائرة إلكترون واحد معدلة تنفذ دائرة محول-رقمى-تماثلى ثمانية بت مع نتائج المحاكاه على الكمبيوتر.

Abstract:
An 8-bit Digital-to-Analog Converter (DAC) based on the Multiple-Value k electron (MVke) Single Electron Circuit (SEC) is presented. With each MVke SEC, a variable number of electrons k*e can be added one by one to an output node. Each MVke SEC, consists of two tunnel junctions and five capacitors. The proposed 8-bit DAC consists of eight MVke SEC blocks in addition to the charge reservoir load capacitor. It is implemented and simulated using SIMON 2.

Keywords:
Single Electron Tunneling (SET), Single Electron Circuit (SEC), Digital to Analog Converter (DAC), Multiple-Value k electron (MVke).

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1. Introduction:

The Single Electron Tunneling (SET) technology is the future technology that is expected to meet the required increase in density and performance and decrease in power dissipation [1-2]. The main device of the SET circuits is the tunnel junction through which individual electrons can move in a controlled manner [3].

A decade ago, the basic physics of SET was well understood and designing useful Single Electron Circuits (SECs) became the important research area [4-5]. In the past few years, some basic building blocks for SEC had been introduced in the literature [6-10].

In this paper, we first briefly discuss the basic physics of SET in section 2. In Section 3, we review a basic SEC building block that was introduced in the literature; the Multiple-Value k electron (MVke) block [3]. Based on the MVke SEC block, we present an 8-bit Digital-to-Analog Converter (DAC) implementation in Section 4. The full design of the 8-bit SEC DAC (inc. detailed schematic diagrams with all parameters for used devices) and simulation results (using the Monte Carlo simulator; SIMON 2 [11]) are included. The conclusions are provided in Section 5.

2. The Basic Physics of SET:

The main component of SEC is the tunnel junction that can be implemented using silicon or metal-insulator-metal structures, GaAs quantum dots, etc.

The tunnel junction can be thought of as a leaky capacitor [11]. For very small tunnel junctions (hence, very small capacitance C_j), the movement of only one electron, from one side of the tunnel junction to the other, may produce a noticeable change e/C of the voltage across the tunnel junction. Note that the above $C = C_j + C_e$ where C_e is the equivalent capacitance of the remainder of the circuit, as viewed from the tunnel junction's perspective.

The discreteness of the electrical charge e leads to the Coulomb blockade effect that is widely known in the field of single-electronics. The critical voltage V_c (the voltage needed in order to make one electron tunnel through the junction) is given by [6]:

$$V_c = e/2C \qquad (1)$$

The Coulomb blockade effect is the suppression of electron tunneling across the tunnel junction at voltages $|V| < e/2C$. This means that for such voltages, there will be no increase in the electrostatic energy of the junction capacitor: $CV^2/2$ (in the case of such increase, the energy would be [4]: $C(V \pm e/C)^2/2$.

Today's well-established technologies uses metal junctions with an area about 50x50 nm^2 that lead to a typical capacitance and its corresponding voltage scale (e/C) in the order of 100 aF and 1 mV, respectively.

To avoid the effects of thermal fluctuations on SEC, the thermal energy k_BT should be much less than the typical one-electron charging energy ($eV = e^2/2C$) [4].

$$k_BT << e^2/2C \qquad (2)$$

The above condition limits the practical use of SEC since the working temp. is restricted to be < 1 K. For a room operating temperature (300 K), junction capacitances should decrease to the range of 0.1 aF. To reach this low capacitance level, the size of the devices should go below few nanometers and single electronics enters the areas of atomic physics and chemistry [4].

3. Review of the MVke SEC Block:

The MVke SEC block [3], shown in Fig. 1, is a SEC basic block with which a variable number of electrons ke can be added to the charge reservoir (CR) output node where k is determined by the input voltage V. The inputs: Enable (E) and Reset (R) are control signals. The MVke block has a dynamic logic behavior, therefore it has to be reset before each new charge transport. This reset can be achieved by setting R = "1" and E = "0".

Considering C = 1 aF as the unit of capacitance for the MVke block, logic "1" = q*e/10*C = 16 mV and logic "0" = 0 V. Let $C_{\Sigma t}$ and $C_{\Sigma i}$ be the equivalent capacitances at internal nodes t and i, respectively [3].

$$C_{\Sigma t} = C_{j1} + C_e + C_v + C_t \quad (3)$$

$$C_{\Sigma i} = C_{j1} + C_{j2} + C_r + C_i \quad (4)$$

In [3], the following values were chosen and/or calculated for the various MVke elements:

$$C_{j1} = C_{j2} = 0.5\ C = 0.5\ aF \quad (5)$$

$$C_{\Sigma i} = 10\ C = 10\ aF \quad (6)$$

$$C_r / C_{\Sigma i} = 5 / 10 \quad (7)$$

$$C_r = 5\ aF \quad (8)$$

$$C_i = 4\ aF \quad (9)$$

$$C_e / C_{\Sigma t} = 5 / 9.5 \quad (10)$$

$$C_{cr} = 10000\ aF = 10\ fF \quad (11)$$

For V = 1, k = C_v / α*C, where α (amplification factor) = 100. Therefore k is determined by C_v. For example, C_v = 300 aF → k = 3.

In [3], an MVke block was simulated (using SIMON [11]) with the following values: C_e = 500 aF, C_v = 300 aF, and C_t = 150 aF. Notice that equation (10) is still valid. It is worth noting here that:

1. Every electron transfer to the charge reservoir output node CR corresponds to an increase of 16 uV in its voltage V_{cr}.
2. V_{cr} maintains its current value when E = R = V = 0 V.
3. V_{cr} maintains its previous value (no charge transport occurs) while E = 0 V (even if input V changes).

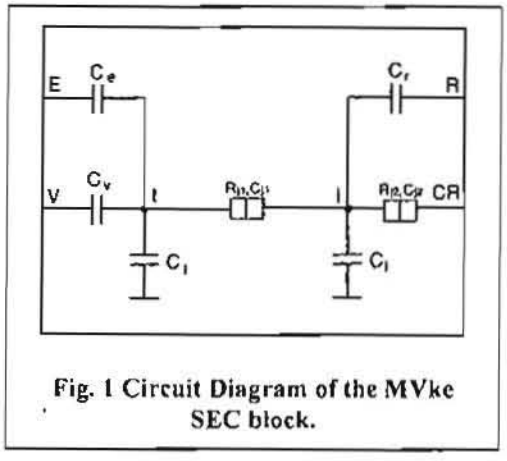

Fig. 1 Circuit Diagram of the MVke SEC block.

4. The 8-Bit DAC SEC:

A. The reported 4-bit DAC SEC:

A 4-bit DAC SEC was implemented using the MVke block. Four MVke blocks were used to implement the 4-bit DAC SEC. For each MVke block, C_v had to be computed for the desired k [3]. All other circuit parameters were kept as presented in Section 3 except for the C_t

values. Keeping C_c = 500 aF, C_t is calculated using the equation C_t = 450 aF - C_v. The calculated values for C_v and C_t are listed in Table 1.

Table 1: The values of C_v for the 4-bit DAC SEC

MVke block	Inputs	k	C_v (aF)	C_t (aF)
1	D0	1	10	440
2	D1	2	20	430
3	D2	4	40	410
4	D3	8	80	370

B. The developed 8-bit DAC SEC:

Using the circuit parameters reported in [3], we were able to extend the DAC design to 6-bit. The 6-bit DAC SEC can be implemented using the values listed in both Table 1 and Table 2.

Table 2: The extra values of C_v for the 6-bit DAC SEC

MVke block	Inputs	k	C_v (aF)	C_t (aF)
5	D4	16	160	290
6	D5	32	320	130

Using the values proposed in [3], we can not extend the DAC design any further (because that value of C_v will need to go beyond the available range of values).

In this paper, we propose the following changes to the original circuit parameters to be able to achieve 8-bit DAC SEC using the MVke SEC block developed in [3]:

1- Increasing the charge reservoir load capacitance C_{cr} value by ten fold to 100 fF.

2- Increasing the C_c value by three folds to 1500 aF and maintaining equation (7) so that we can achieve 8-bit DAC SEC. C_t is calculated using the equation C_t = 1350 aF - C_v. The new values for C_v and C_t are listed in Table 3.

Table 3: The values of C_v for the 8-bit DAC SEC

MVke block	Inputs	k	C_v (aF)	C_t (aF)
1	D0	1	10	1340
2	D1	2	20	1330
3	D2	4	40	1310
4	D3	8	80	1270
5	D4	16	160	1190
6	D5	32	320	1030
7	D6	64	640	710
8	D7	128	1280	70

The schematic diagram of the proposed 8-bit DAC SEC is shown in Fig. 2. The detailed 8-bit DAC SEC (using the circuit parameters listed in this paper) was implemented and simulated using SIMON 2 [11]. Various 8-bit numbers are considered as input to the proposed 8-bit DAC SEC.

Fig. 3 shows the simulation results of the proposed 8-bit DAC SEC for a selected series of 20 input samples using SIMON 2 [11]. Table 4 shows the charge

reservoir output voltage V_{cr} for the selected series of 8-bit inputs.

It should be noted here that E must equal "1" so that digital-to-analog conversion is performed. Otherwise (i.e., E="0"), the charge reservoir remains in the neutral state (i.e., the output voltage V_{cr} equals "0". This can be noticed by looking into the reported values in the rows representing the input samples 12 and 20 within Table 4.

Since we have 8-bit DAC, input can have 256 integer values starting from 0 to 255. It can be noticed from Table 4 that for each increase of 1 in the input, the charge reservoir output voltage V_{cr} increases by 1.6 μV. There will also be a decrease of 1.6 μV in the charge reservoir output voltage V_{cr} for each decrease of 1 in the input.

Both Table 4 and Fig. 3 indicate that the proposed 8-bit DAC SEC performs the correct conversions for both increasing and decreasing inputs. This can be attributed to the introduction of the reset (R) signal (R = "1") before applying any new input sample.

It should be noted here that by reducing the charge reservoir capacitance value C_{cr} , the corresponding voltage V_{cr} increases. For example, when C_{cr} = 4 fF is used, a step increase of about 40 μV is achieved (rather than the 1.6 μV that was achieved when C_{cr} = 100 fF is used. This has the effect of increasing the maximum charge reservoir output voltage V_{cr} from about 400 μV to about 8.4 mV as can be seen in Fig. 4. This came at the expense of having smaller voltage steps for higher bit representations (i.e. the charge reservoir output voltage V_{cr} tends to saturates when input increases). For example, instead of getting 10.2 mV for the maximum input representation, we only get 8.4 mV.

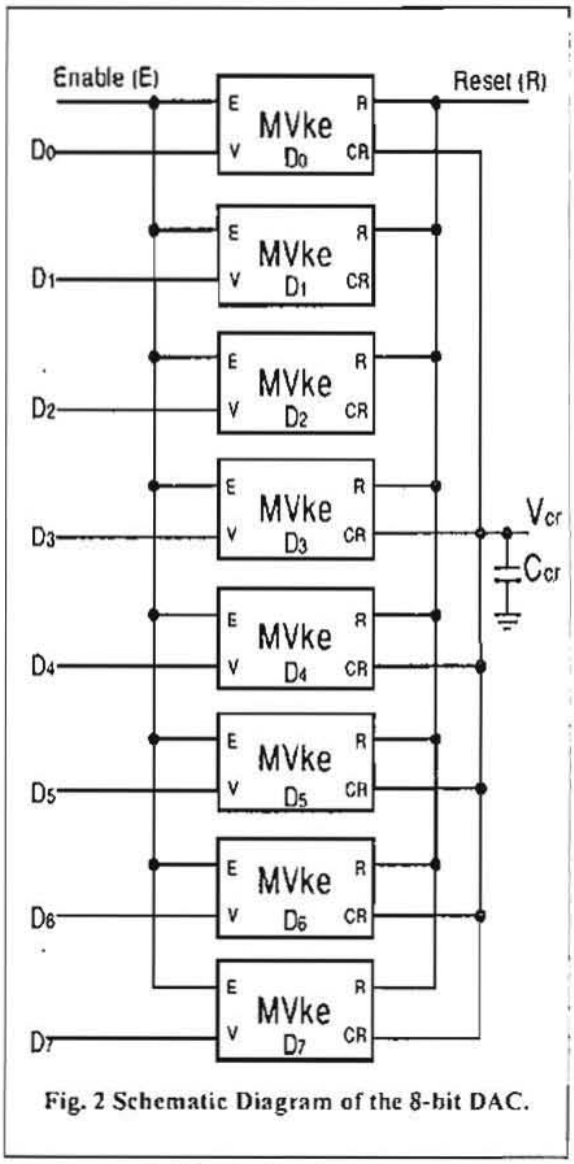

Fig. 2 Schematic Diagram of the 8-bit DAC.

5 Conclusions

In this paper we reviewed the MVke SEC block and the design of a 4-bit DAC that was introduced in [3] using this block. It was shown that using the circuit parameters suggested in the above reference, the DAC design can be expanded to only 6-bit. We introduced some modifications to circuit parameters in order to be able to achieve 8-bit DAC SEC.

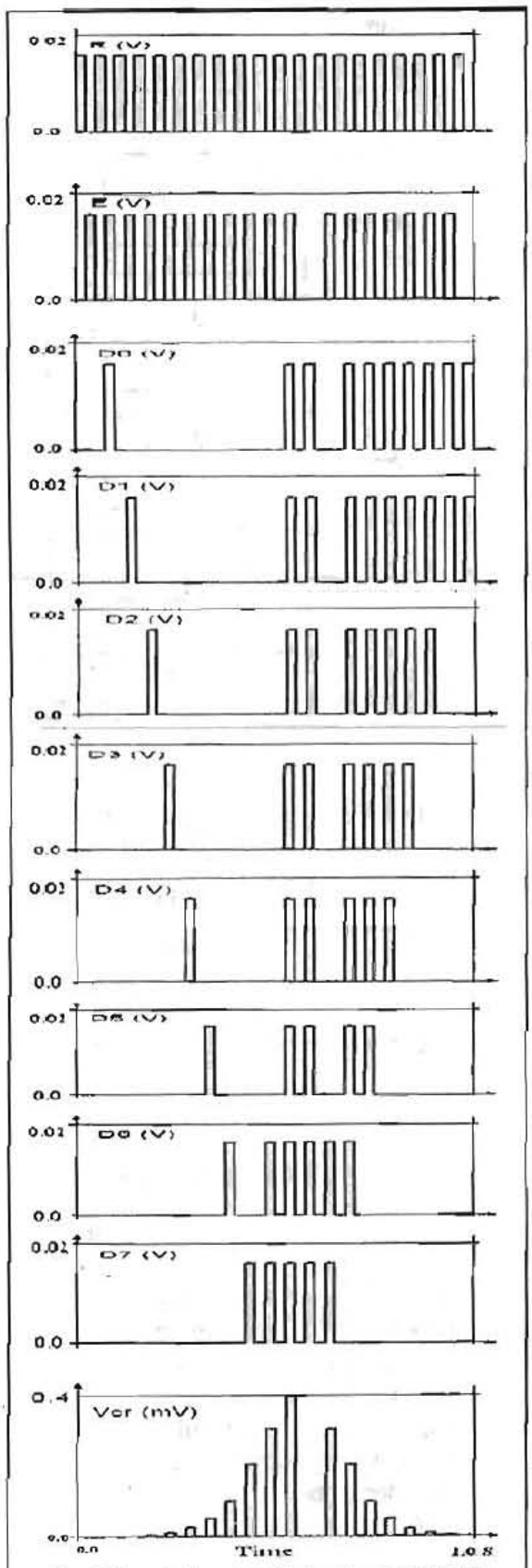

Fig. 3 Simulation results for the 8-bit DAC.

Table 4: The values of V_{cr} for the 8-bit DAC SEC

Sample	8-bit Input	Enable (E)	V_{cr} (μV)
1	0	"1"	0.017
2	1	"1"	1.619
3	2	"1"	3.221
4	4	"1"	6.425
5	8	"1"	12.834
6	16	"1"	25.651
7	32	"1"	51.285
8	64	"1"	102.553
9	128	"1"	203.486
10	192	"1"	304.420
11	255	"1"	397.343
12	**255**	**"0"**	**0.00358**
13	192	"1"	304.420
14	127	"1"	203.486
15	63	"1"	100.951
16	31	"1"	49.683
17	15	"1"	24.049
18	7	"1"	11.232
19	3	"1"	4.823
20	**3**	**"0"**	**0.00004**

The proposed 8-bit DAC SEC consists of 57 circuit elements; 16 tunnel junctions, 40 capacitors, in addition to

the charge reservoir capacitor. The proposed 8-bit DAC SEC was implemented and simulated using the SIMON 2 simulator. We discussed the trade off when changing the charge reservoir capacitance value C_{cr} on the corresponding voltage V_{cr}.

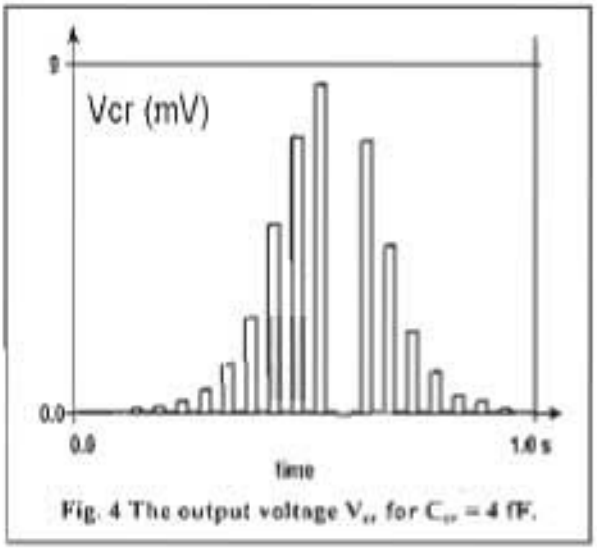

Fig. 4 The output voltage V_{cr} for C_{cr} = 4 fF.

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