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Design and Implementation of a Single-Phase Direct Buck AC-AC Converter with a Minimum Number of Components

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ABSTRACT

A single-phase direct pulse width modulation (PWM) AC-AC converter is proposed in this paper. The proposed converter has a simple structure and efficient performance to be utilized as an AC voltage buck converter. It is designed with a low number of semiconductor switches and passive components (four switches, one inductor, and one capacitor). The major advantages of the proposed converter can be mentioned as: Only one switch operates during each mode of operation decreasing the circuit losses. It is operated with simple pulse width modulation control and doesn't require a safe-commutation strategy. It does not suffer from input source shoot-through and dead time problems. It retains the common sharing ground of the input and output and can be utilized for voltage sag and swell compensation. Additionally, the proposed converter features are high efficiency, continuous input and output currents, and low filtering requirements. The performance of the proposed circuit is extensively evaluated by using MATLAB/Simulink environment. Moreover, a DSP-based laboratory model is built for physical realization of the proposed converter operation.

Keywords*: Direct PWM AC-AC converter; buck converter; continuous current; total harmonic distortion*

1. Introduction

The AC-thyristor voltage controllers that were employing the phase angle control have traditionally been used in industrial applications to achieve the AC-AC conversion. These circuits have many drawbacks such as low input power factor, large total harmonic distortion, low efficiency, and the need for large passive filters. In recent years, this AC-voltage controllers are replaced by the pulse width modulation (PWM) AC-AC converters which have the following features: higher efficiency, better power factor, lower harmonics, ease of control and smaller input/output filter requirements [1,2].

The popular topologies of AC-AC power converters are indirect AC-AC converters with DC link, direct AC-AC converters, and matrix converters. Both the indirect and matrix converters offer adjustable output voltage and frequency. The direct converters are preferred with applications that require only output voltage regulation because of its smaller size, and single stage conversion with high efficiency. Direct AC-AC converter topologies differ from each other in the main function of step up (boost converter), step down (buck converter), or both step up and down (buck-boost converter). Simple structure, uncomplicated control, and high conversion efficiency made the direct AC-AC converter studied continuously.

In [3-7] the AC-AC converters based on the impedance source networks (the Z-source AC-AC converters) can both buck and boost the input voltage but their use is less attractive because they require more passive components and suffer from higher current following through the active switches during shoot through. The z-source AC-AC converters in [3] suffer from commutation problems. The converter in [6] solves the commutation problem and the high voltage spikes on the switches by using a safe-commutation strategy.

The AC-AC converters in [8],[9] requires a greater number of inductors that increase the cost and the overall size. A modification of [9] is developed in [10] by using only two discrete inductors while keeping the same semiconductors count. The AC-AC converters in [9],[10] have a large number of switches conducting

simultaneously and requires bulky input and output filters that limit the efficiency and increase the overall size of the circuit. In [11] two AC-AC converters are developed from the main circuit of [10] by adding series z-source and reduce the number of conducting semiconductors in each mode by using a modified switching strategy. The two converters of [12],[13] suffer from discontinuous input and output currents and require bulky input inductor and bulky input and output capacitors. In addition to the high number of semiconductor switches required by each converter.

The converter introduced in [14] has semicontinuous input and output currents. It requires a large number of switches and diodes. It also needs for a safe-commutation strategy.

The two converters in [15],[16] have high efficiency, quasi-continuous input and output currents, and a lower size of reactive components. Both the two converters employ a high number of semiconductors and a high number of reactive components. In addition to a high number of semiconductors operated with high frequency in each mode of operation that increasing the circuit losses. In reference [17], a single-phase direct buck AC-AC converter for grid voltage compensation is introduced. It is implemented by a six semiconductor switches, six diodes, one inductor, and one capacitor.

A proposed AC-AC converter with simple structure and efficient performance is introduced in this paper. It requires minimum number of components than the competitors. It is designed with one main inductor, one main capacitor, and four semiconductor switches. It doesn't suffer from input source shoot-through and dead time problems. The proposed converter can be utilized for voltage sag and swell compensation as it has a common sharing ground between the input and the output, and the source always feeds the load.

2. Proposed AC-AC Converter

2.1. Circuit Topology

Figure (1) shows the circuit configuration of the proposed AC-AC converter. It consists of four switches S_1 - S_4, one inductor (L_1), and one capacitor (C_1). It operates as a voltage buck converter without any risk of the input source shoot-through. The required input inductor and output capacitor filters are represented by L_{in} and C_{out} respectively.

2.2. Switching Strategy:

The proposed converter is operated with simple pulse width modulation control. The PWM signals are generated by a conventional carrier-based pulse-width modulation (PWM) method as shown in Figure (2). The PWM signal goes to gates of S_1 and S_2 while its complement goes to gates of S_3 and S_4. There are two modes of operation during each half cycle. While each mode, there is only one switch is ON and the body diode of another switch provides the current path.

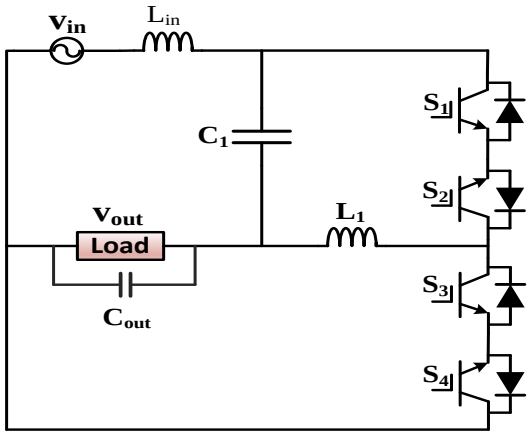


Figure 1- Proposed single-phase direct AC-AC buck converter.

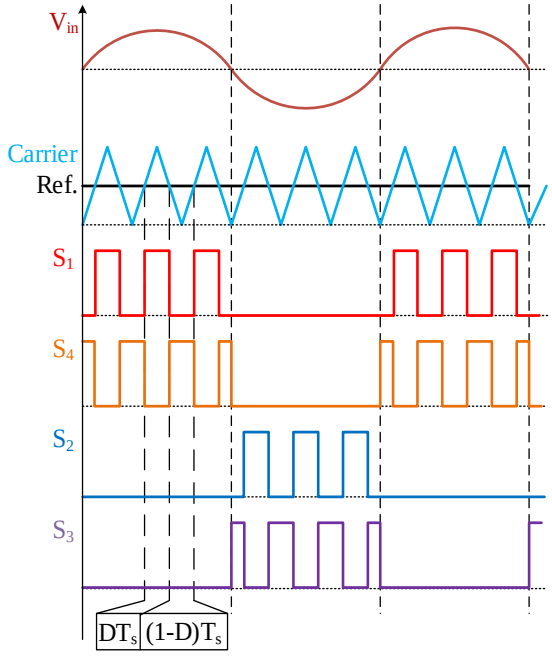


Figure 2- Gating signals of the proposed converter.

2.3. Modes of Operation

I) During the positive half cycle of the input voltage:

a) Mode 1 [0 - DT_s]:

During this mode of operation, the switch S_1 is ON and the body diode of S_2 is forward biased for an interval DT_s. The capacitor C_1 discharges its stored energy while the inductor L_1 is charged from the source and

the capacitor C_1 as shown in Figure (3.a). The voltage mathematical equations of mode 1 will be written as

$$v_{L1} = v_{C1} \quad (1)$$

$$v_{C1} = v_{in} - v_o \quad (2)$$

Where v_{in} represents the input voltage and the voltage drop across the input filter inductor (L_{in}) is neglected, v_o is the output voltage, and D is the duty ratio.

b) Mode 2 [DTs - Ts]:

During (1-D) T_s interval, as shown in Figure (3.b), only the switch S_4 is ON and the body diode of S_3 is forward biased. The inductor L_1 discharges its stored energy into the load while its current decreases through the path formed by S_4 and the body diode of S_3. The capacitor C_1 is recharged from the source. The voltage across the inductor is calculated for this mode of operation as

$$v_{L1} = -v_o \quad (3)$$

$$v_{C1} = v_{in} - v_o \quad (4)$$

By applying the volt-second balance condition on the voltage across the inductor (L_1) from equations (1) and (3), the voltage gain (G) of the proposed converter is calculated by

$$G = \frac{v_o}{v_{in}} = D \quad (5)$$

During each mode of operation, there is a path for the input current to flow through therefore, it has a continuous waveform that indicates a high current quality.

II) During the negative half cycle of the input voltage:

The operation principles of the proposed converter are the same as that in the positive half cycle. The main difference is the switch S_2 is operated with the body diode of S_1 then S_3 is operated with the body diode of S_4 as shown in Figures (3.c and 3.d).

a) Mode 3 [0 - DTs]:

During this mode of operation as shown in Figure (3.c), the switch S_2 is ON and the body diode of S_1 is forward biased. The inductor L_1 is charged from the source and the capacitor C_1.

b) Mode 4 [DTs - Ts]:

In this mode as shown in Figure (3.d) the inductor L_1 discharges its stored energy into the load through the path formed by S_3 and the body diode of S_4.

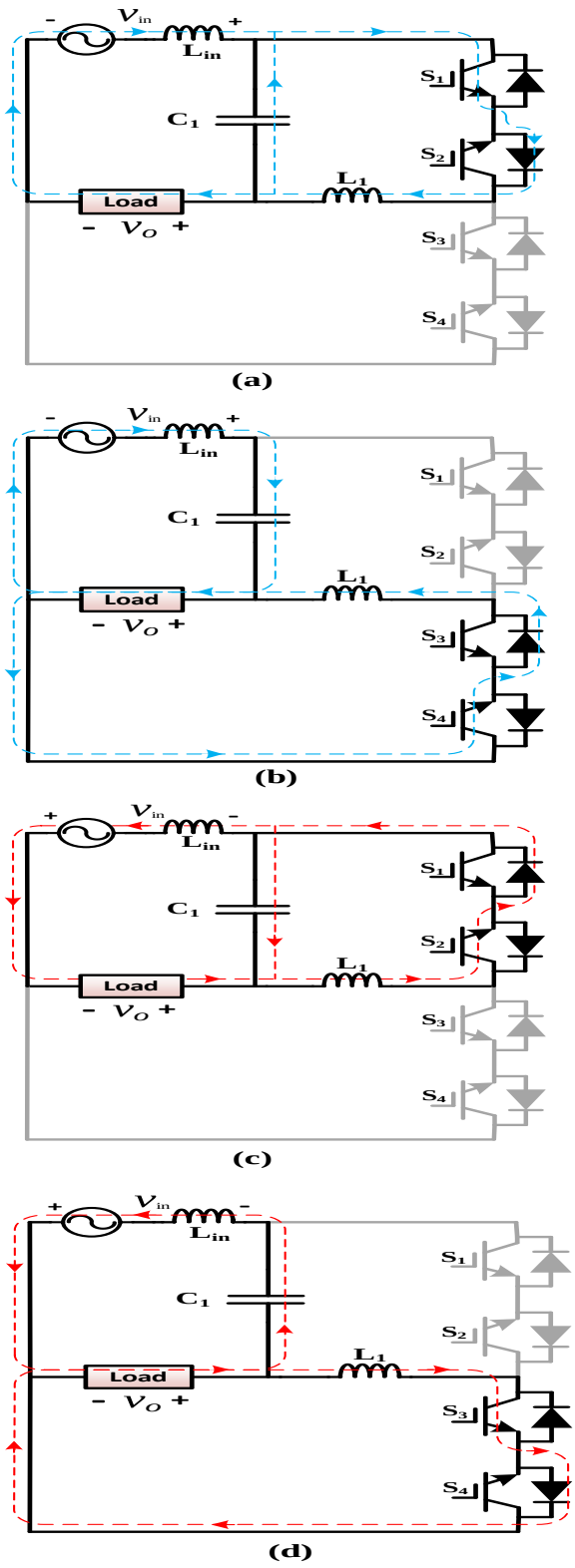


Figure 3-Modes of operation of the proposed AC-AC converter (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4.

3. Parameter's Design of The Proposed Converter

The passive components of the power electronics converter are mainly designed by considering their maximum tolerable current and voltage ripples. The inductor current ripple and capacitor voltage ripple can be acquired from the following equations

$$v_l = L \frac{\Delta i_l}{\Delta t} \quad (6)$$

$$i_c = C \frac{\Delta v_c}{\Delta t} \quad (7)$$

The inductor maximum tolerable current ripple is taken as a factor α% from its maximum current I_l^{max}. From equations (1) & (6) and for maximum current handling requirement I_l^{max} nearly equal I_o the inductor equation will be as follow

$$L_1 = (1 - D)\, D^2 \frac{{V_{in}}^2}{\alpha\, f_{sw}\, P_o} \quad (8)$$

The capacitance C_1 will be calculated for a maximum voltage ripple of β% ($\Delta v_c = \beta\, v_c$). Considering ideal circuit and from equations (4) & (7) the capacitance value C_1 is given by

$$C_1 = \frac{P_o}{\beta\, f_{sw}\, {V_{in}}^2} \quad (9)$$

Where P_o and f_{sw} are the output power and the switching frequency respectively.

To select the required ratings of the semiconductors of the proposed converter, the peak voltages and currents of the semiconductor switches are calculated from equations (10) and (11).

$$V_{S1-S4\,(pk)} = \sqrt{2}\ V_{in-rms} \quad (10)$$

$$I_{S1-S4\,(pk)} = \sqrt{2}\ I_{o-rms} \quad (11)$$

4. Calculation of Power Losses and Efficiency for The Proposed Converter

4.1. Calculation of semiconductor switch power losses

Conduction losses, switching losses, and blocking losses represent the power losses of any semiconductor switch, IGBT or diode. The blocking losses are low compared to the other two parts and can be neglected [18].

(a) Conduction losses

The IGBT instantaneous conduction losses ($P_{cond.IGBT}$) are given by

$$P_{cond.IGBT}(\mathrm{t}) = V_{CE0}\,.\,i(t) + R_{\mathrm{C}}\,.\,i(t)^2 \quad (12)$$

Where V_{CE0} is the zero-current collector-emitter voltage during on-state, R_C is the collector-emitter resistance during on-state, and *i*(t) is the instantaneous current following through the IGBT.

There is only one IGBT operating in each mode of operation, so the conduction losses for the four IGBTs is equivalent to the conduction losses of a one IGBT if it is continuously operating during the full cycle. The IGBT current is the same as the inductor current (i_{L1}), Thus the average value of conduction losses can be given as:

$$P_{cond.IGBT\ avg.} = \frac{1}{\pi}\int_0^{\pi}[V_{CE0}\,.\,i(t) + R_{\mathrm{C}}\,.\,i(t)^2]d(wt) = V_{CE0}\,.\,I_{avg} + R_{\mathrm{C}}\,.\,{I^2}_{rms} \quad (13)$$

Where I_{avg}, I_{rms} are the average and RMS values of the switch current. Similarly, the average conduction losses of the diode are given as:

$$P_{cond.D.avg.} = V_{D0}\,.\,I_{avg} + R_{\mathrm{D}}\,.\,{I^2}_{rms} \quad (14)$$

Where V_{D0} is the diode zero-current voltage and R_D is the diode on-state resistance.

There is only one IGBT and one diode in the current path during each state of operation. Thus, the total conduction losses can be expressed as:

$$P_{cond.total} = P_{cond.IGBT\ avg.} + P_{cond.D.avg.} \quad (15)$$

(b) Switching losses

The switching losses of the switch (P_{sw}) can be expressed as:

$$P_{sw} = \left(W_{\mathrm{on}} + \mathrm{W}_{off}\right).F_{\mathrm{sw}} \quad (16)$$

Where W_{on} and W_{off} are the energy dissipated during turn-on and turn-off times, respectively. There are two switches operates respectively during each half cycle so, the average switching losses for the proposed converter equal the sum of the switching losses for the two switches considering that they are turned on and off along the overall cycle.

$$P_{sw.avg} = 2.(P_{sw}) \quad (17)$$

4.2. Calculation of efficiency

The converter output power can be expressed as:

$$P_o = R_{\mathrm{o}}\,.\,{I^2}_{o-rms} \quad (18)$$

The converter power losses are the summation of the losses in the switches given by equations (15) and (17), with neglecting the power losses in the passive components.

$$P_{Converter\ losses} = P_{cond.total} + P_{sw.avg} \quad (19)$$

The converter input power can be expressed as:

$$P_{in} = P_o + P_{Converter\ losses} \quad (20)$$

The percentage efficiency of the converter can be calculated from equations (18) and (20) as:

$$Efficiency\ \% = \frac{P_o}{P_{in}} \times 100 \quad (21)$$

The total harmonic distortion will be measured and calculated by using the MATLAB fast Fourier transform (FTT) analysis.

5. Simulation Results

The validity of the proposed converter is extensively evaluated by using the MATLAB/Simulink environment. The proposed circuit performance is

obtained and evaluated at high switching frequency (f_{sw}) equals 60 KHz, and at low switching frequency equals 2 KHz. The high switching frequency gives an excellent performance with a small passive components and low input/output filtering requirements that means small converter size, so the proposed converter is designed at 60 KHz. The low switching frequency is chosen based on the sampling rate of the control board used in experimental setup as the drive circuit in the laboratory can operate with a maximum frequency 2 KHz.

Table 1- Converter's parameter values at different switching frequency

parameters	f_{sw} = 60 KHz	f_{sw} = 2 KHz
Capacitor (C_1)	1.5 µF	5 µF
Inductor (L_1)	0.45 mH	13.5 mH
Input inductor (L_{in})	1 mH	10 mH
Output capacitor (C_{out})	2 µF	10 µF
Input voltage (V_{in})	110 V_{rms} /50Hz	
Resistive load (R_o)	50 Ω	
Inductive load (R_o & L_o)	50 Ω & 100 mH	

The converter parameters at the two switching frequencies are summarized in table (1). As illustrated in equations (8) and (9) the switching frequency has a main role in the design of the converter parameters. The converter parameters at high switching frequency are smaller than at low switching frequency for the same input voltage and circuit performance.

5.1. Circuit Performance at High Switching Frequency

The circuit performance for the proposed converter when operated at high switching frequency f_{sw} = 60 KHz is validated by the following figures. The system is supplied by a 110 V-rms AC supply and connected to a resistive load (R_o=50 Ω). Figure (4) shows the waveforms of the input and output voltages and currents when the duty ratio is set as D=0.7. It indicates that the peak output voltage shown in figure (4.b) equals 109 V for a peak input voltage of 155.5 V with voltage gain of (G = 0.7). From Figures (5.a & 5.b), it is noticed that while the inductor current i_{L1} increases, the capacitor voltage v_{c1} decreases as illustrated in mode 1 of operation, and while the inductor current i_{L1} decreases, the capacitor voltage v_{c1} increases as illustrated in mode 2 of operation. As shown in Figures (5.c & 5.d), the voltage stresses across S_1 and S_2 nearly equal the input voltage as indicated from equation (10). The MATLAB Fast Fourier transform (FTT) analysis also shows that the THD of the output voltage waveform and the input current waveform equal 0.8% and 0.3% respectively as shown in Figure (6).

From calculation of the output power and power losses as indicated in the numerical analysis, the converter efficiency nearly equals 97 % at D=0.7 and f_{sw} = 60 KHz. Figures (4-6) validate that the input and output currents are continuous waveforms and have better current quality and low THD.

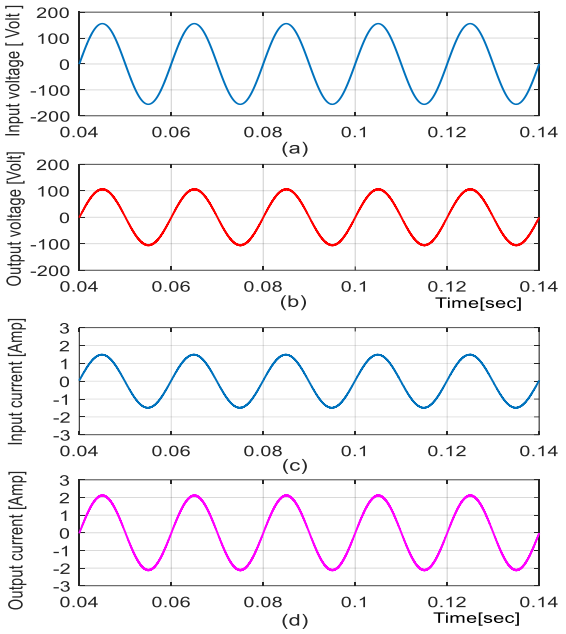


Figure 4- Simulation results of the proposed converter at D=0.7 and f_{sw} =60 KHz feeding a resistive load. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current.

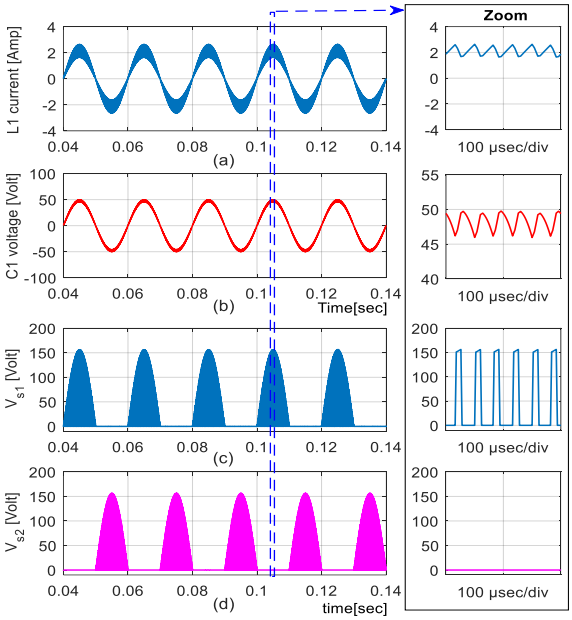
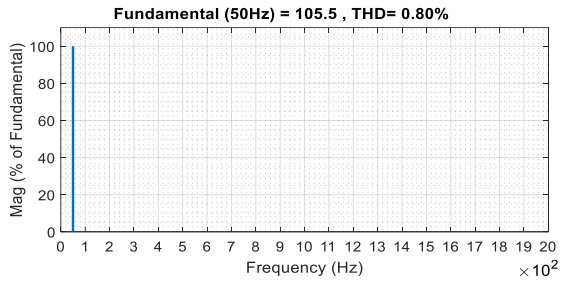
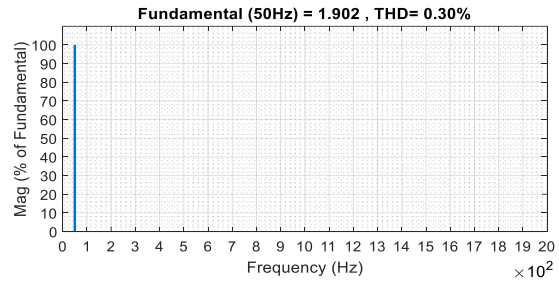


Figure 5- Simulation results of the proposed converter at D=0.7 and fsw =60 KHz feeding a resistive load. (a) Inductor (L1) current. (b) Capacitor (C1) voltage. (c)&(d) Voltage stresses across S1 and S2.



(a)



(b)

Figure 6- THD for the proposed converter at f_{sw}=60 KHz. (a) Output voltage. (b) Input current.

5.2. Circuit Performance at Low Switching Frequency

The circuit performance for the proposed converter when operated at low switching frequency f_{sw} = 2 KHz is validated by the following figures. The converter is supplied by a 110 V-rms AC supply and connected to a resistive load (R_o=50 Ω). From Figure (8.b) the peak output voltage equals 77 V, and the voltage gain is 0.5. As shown in Figures (8 and 10), the circuit performance at low switching frequency is the same as at high switching frequency after changing the converter parameters values.

Figure (11) shows the harmonic spectrum of the output voltage and input current for the proposed converter at f_{sw} =2 KHz. The THD for the output voltage and the input current equal 4.27% and 5.16% respectively. The THD is in acceptable limit and indicates the high quality of the converter.

The simulation results of the proposed converter when operated at f_{sw}=2 KHz and connected to an inductive load (50 Ω and 100 mH) listed with system parameters in table (1) are shown in Figures (14 & 15). For a peak input voltage of 155.5 V, the peak output voltage is 77.7 V, and the voltage gain equals 0.5.

6. Experimental Results

The proposed converter is designed, built, and tested in the laboratory to verify its operation. An experimental setup is implemented as shown in Figure (7) with components listed in table (2). The experimental results are obtained at f_{sw}=2 KHz based on the sampling rate of the IGBT drive circuit used in experimental setup. The electrical specifications of the prototype at low switching frequency are shown in table 1. The active switches (S_1-S_4) are represented by two modules of MITSUBSHI CM100DY-24H IGBTs. A digital signal processor dSPACE (DS-1104) system is used to design the control circuit and generating the PWM signal. Then , the PWM signal is sent to a drive circuit to amplify the voltage of the IGBTs pulses taken from the dSPACE (DS-1104) platform, and to isolate the control system from the power system.

A signal transducer's kits are used to measure the circuit current via LA25-NP current sensor and the circuit voltages via LV25-P voltage sensors. The measured currents and voltages are sent to dSPACE (DS-1104) platform via DSP Analogue to Digital interface.

Figure 7-Experimental setup for the proposed converter.

Table 2- Experimental Components

No	Component	No	Component
1	dSPACE (DS1104) platform	7	Load Resistor (R_o)
2	2 IGBTs modules (MITSUBSHI CM100DY-24H)	8	Autotransformer
3	Drive circuit	9	Transducer Kit
4	Inductor (L_1)	10	Computer
5	Input filter Inductor (L_{in})	11	Measurement device
6	Capacitors Box (C_1 & C_{out})		

For resistive load, the experimental input voltage, output voltage, input current and output current waveforms are shown in Figure (9). The voltage gain is G=0.482 for an input voltage 110 V-rms. The efficiency of the converter is calculated as indicated in section (4) and equals 95% at D=0.5 and f_{sw} =2KHz. Figure (12) shows the inductor (L_1) current, capacitor (C_1) voltage and voltage stresses across the switches S_1 and S_2. As seen from these figures, the experimental results are in a good agreement with the simulation results. Also, the peak values of the voltages across the switches are in a good agreement with the calculated value from equation (10). It is observed from Figure (13) that the THD of input voltage, output voltage, and input current are within acceptable limits.

The difference between the experimental and the simulation results is a low voltage stress appears across the switch during its turn off state, due to the internal characteristics of its antiparallel diode.

When the input voltage is 110 V-rms and R_o is 50 Ω, the efficiency of the proposed converter varies with the variation of duty ratio. The peak efficiency of 96.8% is read for the proposed converter when the duty ratio is 0.25. The minimum efficiency of the proposed converter equals 94.6% when the duty ratio is 0.8. Moreover, for the whole range of duty ratio variations, the efficiency of the proposed converter is more than 94.6% for almost the same input voltage and the same load. Mainly, the aforementioned high efficiencies offered by the proposed converter are the results of the lower number of the employed semiconductor switches and passive components.

To validate the ability of the operation of the proposed converter with inductive loads, the experimental results are provided for the proposed converter when connected with an inductive load (50 Ω and 100 mH) given in table 1. The experimental waveforms are shown in Figures (16 and 17). These figures indicates that the proposed converter operates with the inductive load with high quality sinusoidal waveforms as well as it operates with the resistive load.

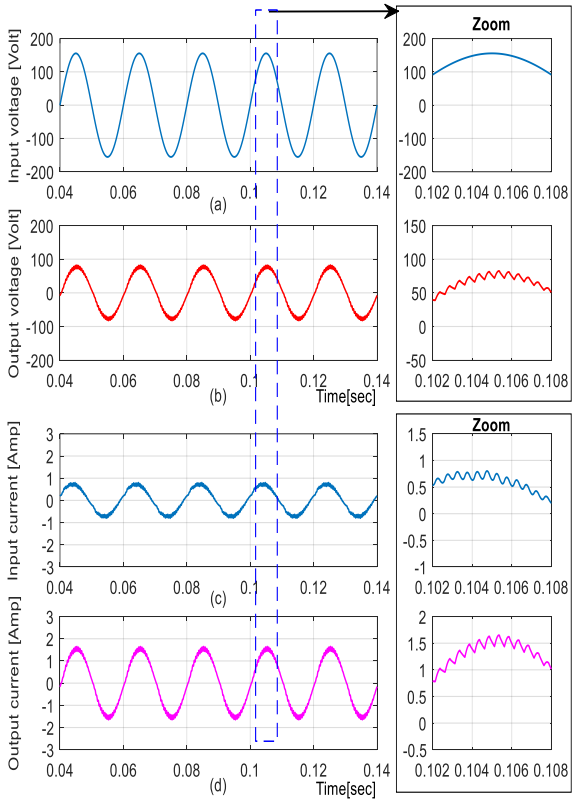


Figure 8- Simulation results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding a resistive load. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current.

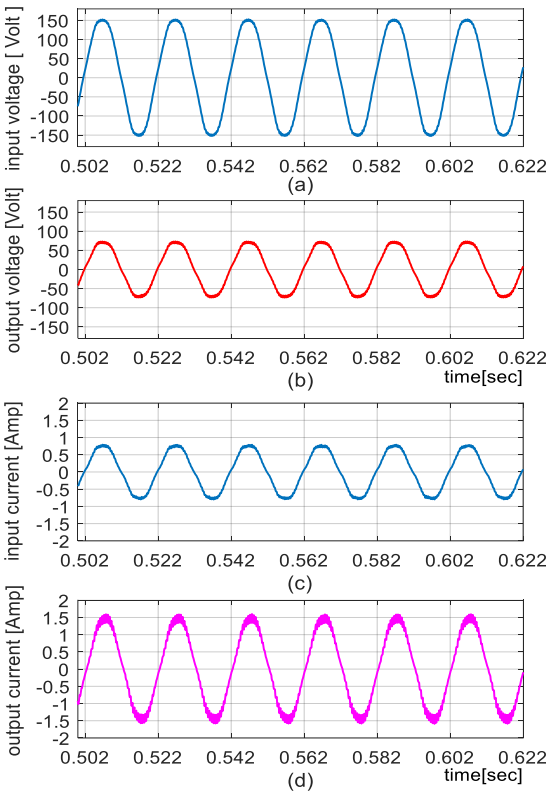


Figure 9- Experimental results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding a resistive load. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current.

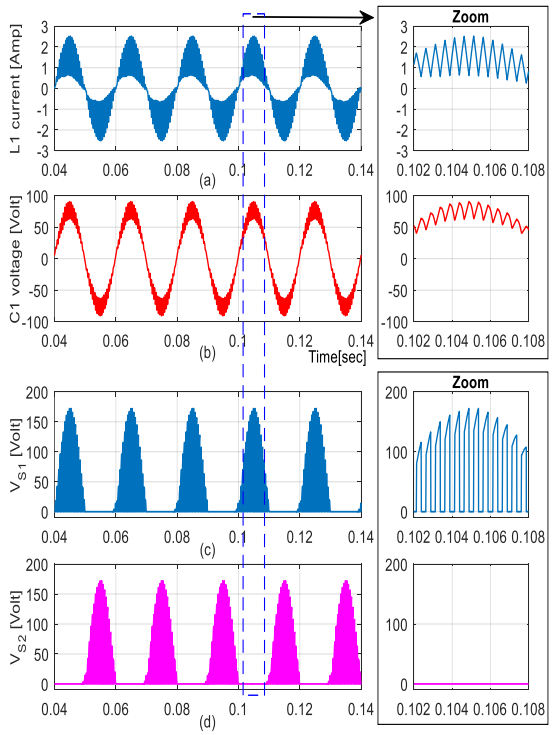


Figure 10- Simulation results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding a resistive load. (a) Inductor (L_1) current. (b) Capacitor (C_1) voltage. (c)&(d) Voltage stresses across S_1 and S_2.

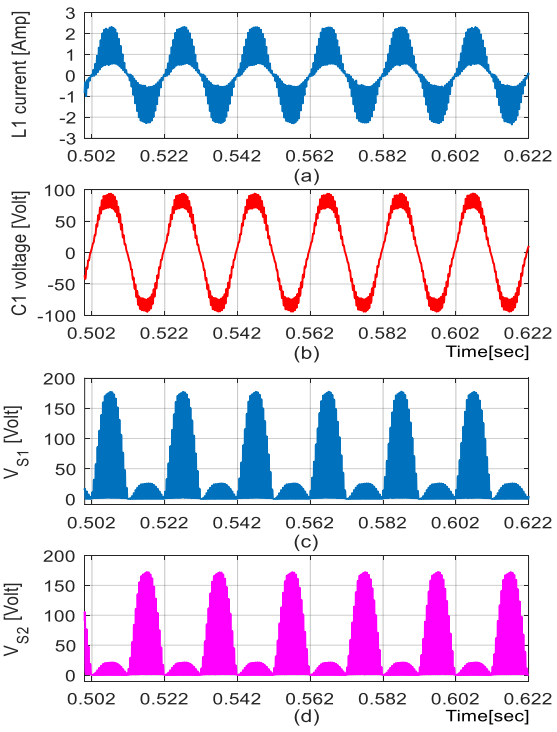


Figure 12- Experimental results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding a resistive load. (a) Inductor (L_1) current. (b) Capacitor (C_1) voltage. (c)&(d) Voltage stresses across S_1 and S_2.

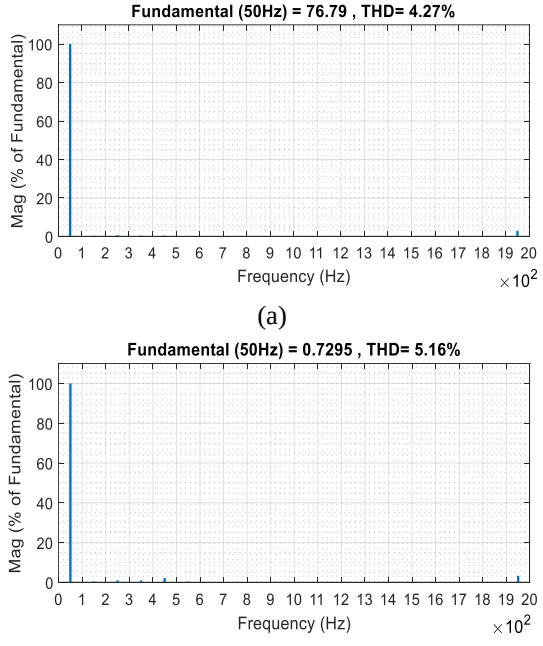


Figure 11- THD for simulation waveforms at f_{sw}=2 KHz and D=0.5. (a) Output voltage. (b) Input current.

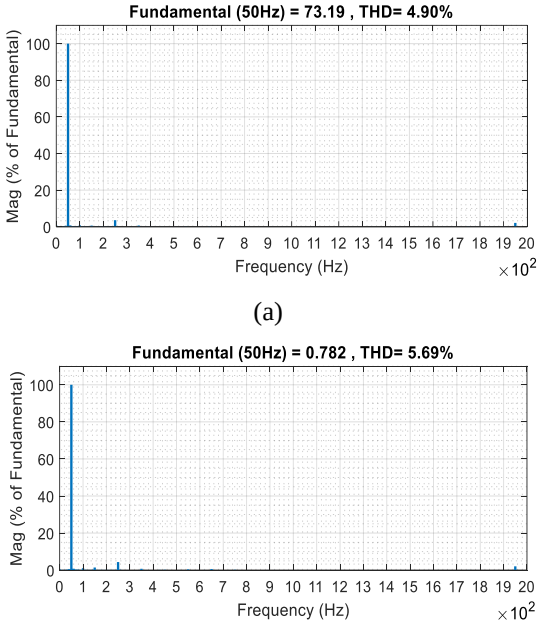


Figure 13- THD for the experimental waveforms at f_{sw}=2 KHz and D=0.5. (a) Output voltage. (b) Input current.

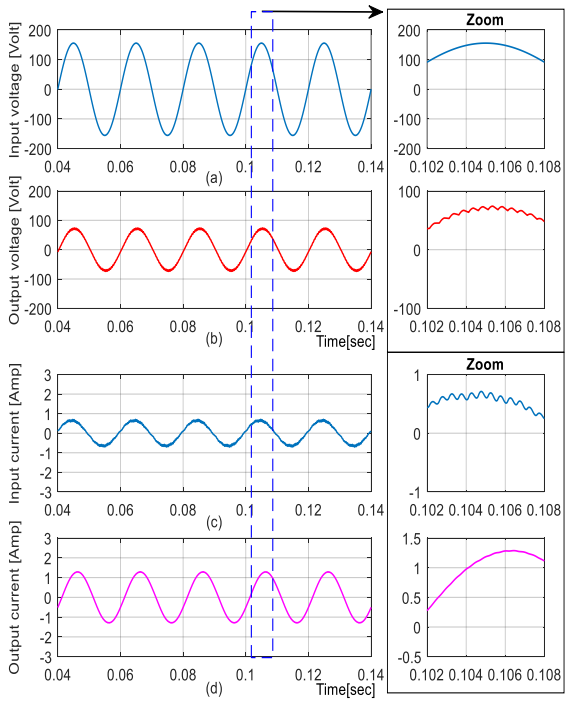


Figure 14- Simulation results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding an inductive load. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current

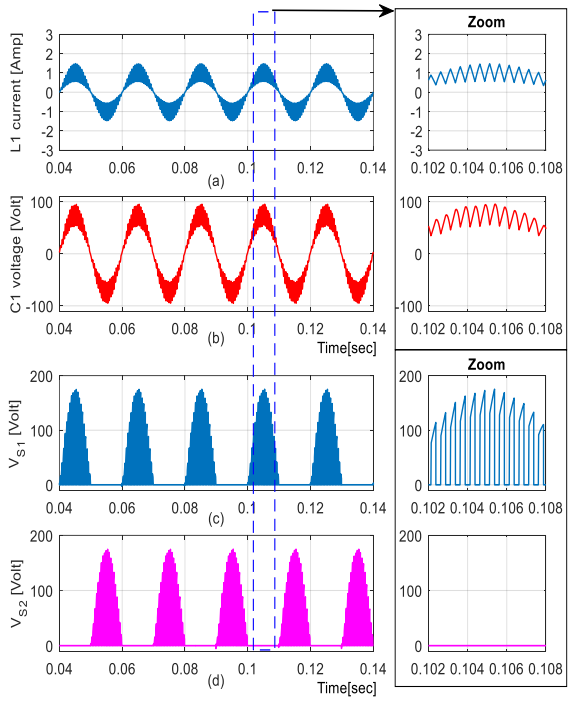


Figure 15- Simulation results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding an inductive load. (a) Inductor (L_1) current. (b) Capacitor (C_1) voltage. (c)&(d) Voltage stresses across S_1 and S_2.

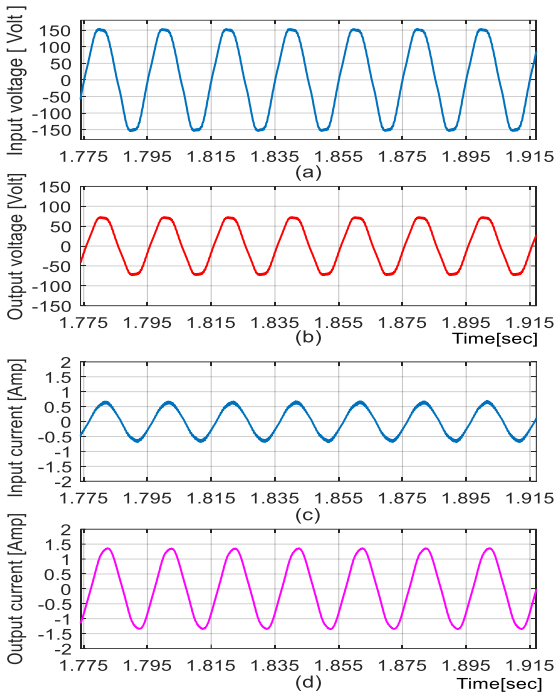


Figure 16- Experimental results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding an inductive load. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current.

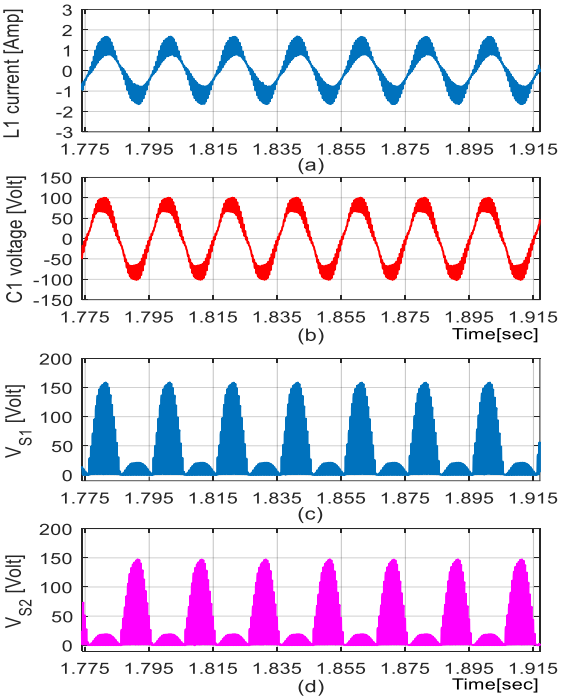


Figure 17- Experimental results of the proposed converter at D=0.5 and f_{sw} =2 KHz feeding an inductive load. (a) Inductor (L_1) current. (b) capacitor (C_1) voltage. (c)&(d) Voltage stresses across S_1 and S_2.

The proposed converter is also tested under closed loop control to validate the dynamic behavior of the proposed converter as shown in Figure (18). The experimental results are recorded when the proposed converter subjected to a step decrease in the reference output voltage. The reference output voltage is decreased suddenly from 70 V-rms to 50 V-rms by using a closed loop control system. The input voltage is remained constant, the input and output currents were decreased as shown in Figure (19). These figures indicate that the transients of the waveforms are damped fast with negligible oscillations.

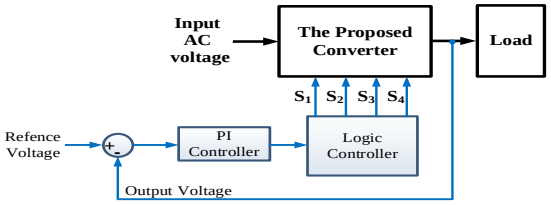


Figure 18- Block diagram for the closed loop system

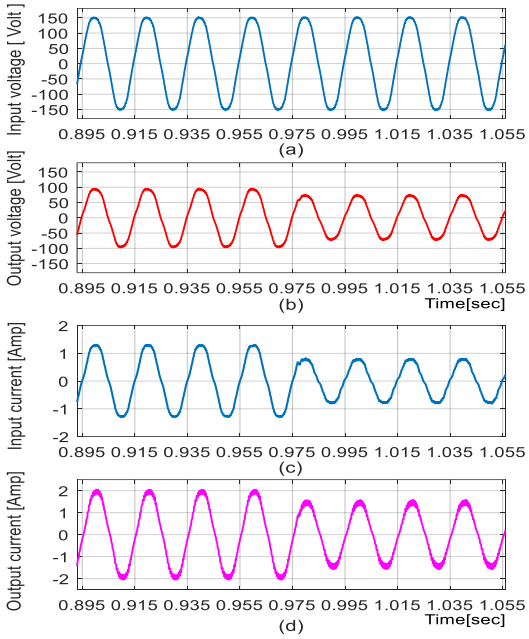


Figure 19- Experimental results of the proposed converter for a step decrease in the reference output voltage at f_{sw} =2 KHz and feeding a resistive load. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current.

The simulation results when the circuit subjected to a decrease in the load resistance from R_o = 50 Ω to R_o = 25 Ω and then retained to 50 Ω are shown in Figure (20). The output voltage is maintained constant at 50 Vrms by using closed loop control. The input and output currents increased as a result to the load resistance decrease.

The experimental results, shown in Figure (21), indicate the response of the proposed converter to a decrease in the resistive load from R_o = 50 Ω to R_o = 25 Ω. The output voltage is maintained constant at 50 V rms. The output current increased as a result to the load decrease. The system has a fast response with negligible oscillations.

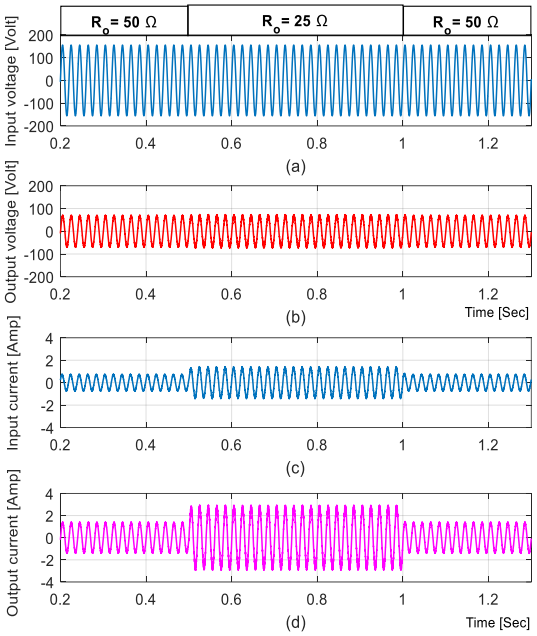


Figure 20 - Simulation results for closed loop dynamic response for a decrease in R_o by 50%. (a) Input voltage. (b) Output voltage. (c) Input current. (d) Output current.

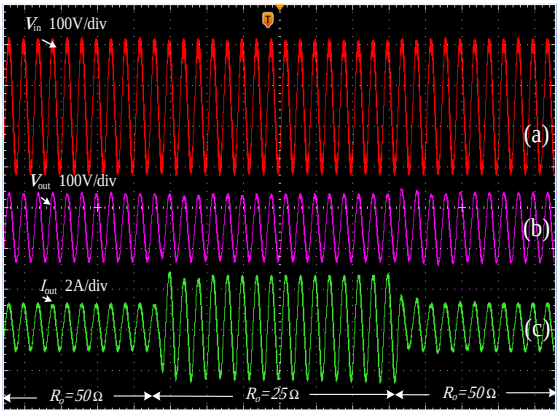


Figure 21- Experimental results for the converter Response to a decrease in the connected load from R_o = 50 Ω to R_o = 25 Ω. (a) Input voltage. (b) Output voltage. (c) Output current.

All the above experimental results are in good agreement with the previous analysis and simulation results, and therefore, validate the features of the proposed AC-AC converter.

7. Comparison Between Various AC-AC Converters

The proposed converter design at high switching frequency is compared with other AC-AC converters as shown in table (3) to validate its features. From table (3) it is concluded that the proposed converter requires lower number of switches, lower number of passive components, and lower filtering requirements than the competitors. The number of switches operated with high frequency, and the number of semiconductors simultaneously conducting during each mode of operation is also minimum. In addition, the proposed converter employs only one inductor and one capacitor.

Table 3- Comparison Between Various AC-AC Converters

Description	Proposed converter	AC-AC Buck Converter of [15]	AC-AC Converter of [10]	AC-AC Converter of [14]	AC-AC Buck Converter of [17]
No. of switches with antiparallel diode	4 ($S_1 – S_4$)	6 ($S_1 – S_6$)	4 ($S_1 – S_4$)	6 ($S_1 – S_6$)	6 ($S_1 – S_6$)
No. of separate diodes	–	–	4 ($D_1 – D_4$)	6 ($D_1 – D_6$)	6 ($D_1 – D_6$)
No. of inductors	1 (L_1)	2 (L_1, L_2)	2 (L_1, L_2)	1 (L_1)	1 (L_1)
No. of energy storing or bypass capacitors	1 (C_1)	2 (C_1, C_2)	(C_1, C_2)	–	1 (C_1)
Commutation problem	No	no	no	no	no
Need soft commutation strategy	No	no	no	yes	yes
No. of switches operating with high switching frequency in each switching cycle	1	2	2	3	2
Continuity of input and output currents	continuous	Quasi-continuous	Quasi-continuous	Quasi-continuous	Quasi-continuous
Required input/output filters	Small L_{in} Small C_{out}	Moderate L_{in} Small C_{out}	Moderate C_{in} Moderate C_{out}	Small C_{in} Moderate C_{out}	Small L_{in} Small C_{out}
Voltage gain $\frac{v_o}{v_{in}}$	D	D	$\frac{D}{1-D}$	D	D

8. Conclusions

In this paper, a single-phase direct buck AC-AC converter, which offers an efficient performance with simple structure is proposed. The proposed converter is implemented with minimum number of components than the competitors that decreases the power losses and the converter size, and also increases its efficiency. It operates as a voltage buck converter with voltage gain equals D. For the whole range of duty ratio variations, the efficiency of the proposed converter is more than 94.6%. The parameters design, analytical studies, and detailed comparison with some recent converters are provided. The performance of the proposed converter at 60 KHz and 2 KHz switching frequency is evaluated by using MATLAB/SIMULINK. An experimental setup is implemented to validate the actual performance of the proposed converter. The simulation and experimental results validate its major features such as : Continuous waveforms of input and output current, high power quality, lower filtering requirements, and high efficiency. Also, The THD of the voltage and current waveforms are in acceptable limit.

9. References

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