Mansoura University Faculty of Engineering Electronics and Communications Engineering Department

Digital Circuits 1 - Term Exam	Exam Time: 3 hours
1st year Communications - 2nd Term	Total Marks: 70 Marks
Exam Date: June 04, 2014	

Important Instructions:

1 This exam contains:

20 Questions (Fill the blanks with pre-selected words) --> Write ONLY your answers in the answer booklet (10 Marks; 0.5 Mark each)

15 MCQs (4 choices each) --> Mark your answer selection in the MCQ answer sheet in the middle of the answer booklet Q1-Q15 (15 Marks; 1 Mark each)

20 Questions (True/False) --> Mark your answer selection in the MCQ answer sheet in the middle of the answer booklet Q16-Q35 (10 Marks; 0.5 Mark each)
Mark ① for TRUE answer and mark ② for FLASE answer.

2 Questions (Regular technical questions) --> Write your answers in the booklet (35 Marks)

My best wishes to YOU!

Dr. Sameh Rehan

Note: This exam has questions on both sides of the questions' sheets.

Answer the following 15 MCQs in the MCQ answer sheet in the answer booklet: (15 Marks)

Q1 A circuit that converts an analog waveform to a digital signal is commonly called a(n) _____.
① PLD ③ DAC
② ADC ④ CAD

Q2 A circuit that is most likely to be found in a CD player is a(n) _____.
① digital-to-analog converter ③ SPLD
② programmable logic device ④ analog-to-digital converter

Q3 When using negative logic _____.
① HIGH = 1 and LOW = 0 ③ HIGH = 0 and LOW = 1
② HIGH = 0 and LOW = -1 ④ LOW = -1 and HIGH = 1

Q4 The math symbol for time of transition from LOW to HIGH is _____.
① t_r ③ t_w
② T ④ t_f

Q5 The math symbol for time of transition from HIGH to LOW is _____.
① t_r ③ t_w
② T ④ t_f

Q6 For a negative-logic pulse, the leading edge is the _____.
① LOW-to-HIGH transition ③ rising edge
② positive-going edge ④ negative-going edge

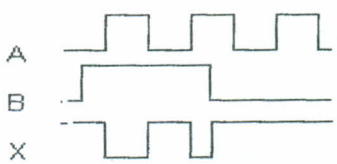
Q7 The output of an AND gate is LOW _____.
① only when all inputs are LOW ③ when at least one input is LOW
② only when all inputs are HIGH ④ no answer is correct

Q8 The output of an OR gate is LOW _____.
① only when all inputs are LOW ③ only when all inputs are HIGH
② whenever any input is HIGH ④ no answer is correct

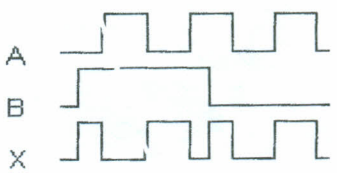
Q9 Two kinds of data selectors are _____ and _____.
① encoders, decoders ③ multiplexers, demultiplexers
② comparators, registers ④ adders, subtractors

Q10 Which converts data from a serial to a parallel form?
① Comparator ③ Encoder
② Demultiplexer ④ Multiplexer

Q11 This is the timing diagram for a 2-input _____ gate.
① AND
② NAND
③ OR
④ NOR



Q12 This is the timing diagram for a 2-input _____ gate.
① AND
② OR
③ XOR
④ XNOR



Q13 This is the truth table for a(n) _____.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

① NAND
② NOR
③ AND
④ OR

Q14 This is the truth table for a(n) _____.

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

① NAND
② NOR
③ AND
④ OR

Q15 This is the truth table for a(n) _____.

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

① NAND
② NOR
③ AND
④ OR

Answer the following 20 TRUE/FALSE questions in the dedicated MCQ answer sheet Q16-Q35 in the answer booklet: **(10 Marks; 0.5 Mark each)**

Q16 6 binary digits are required to count to decimal 100.
Q17 In binary addition, 10 + 11 = 21.
Q18 In binary multiplication, 11 × 11 = 1001.
Q19 In binary division, 1000 ÷ 0100 = 100.
Q20 In binary subtraction, 101-11 = 10.
Q21 The decimal number system consists of the digits 0-10.
Q22 The largest numerical value that is possible with a 4-bit binary number is 16.
Q23 The largest single digit in the octal numbering system is 7.
Q24 A circle, or bubble, on a distinctive-shape logic symbol indicates a logic inversion.
Q25 The OR gate performs as switches wired in series.

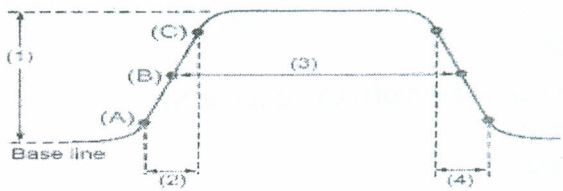
Q26 The output of a 2-input XNOR gate is 1 when the inputs are equal, or identical.
Q27 The output of an AND gate is HIGH only when all inputs are HIGH.
Q28 When the inputs to a 3-input OR gate are 001, the output is 1.
Q29 When the inputs to a 3-input NAND gate are 001, the output is 1.
Q30 When the inputs to a 3-input NOR gate are 001, the output is 1.
Q31 The XOR gate can be used to add two bits.
Q32 DeMorgan's theorem states that: $\overline{XY} = X+Y$
Q33 The commutative law of Boolean addition states that A + B = A . B.
Q34 The Karnaugh maps provide `cookbook` approaches to simplifying Boolean expressions.
Q35 When grouping cells in a Karnaugh map, the cells must be combined in groups of 2's.

Fill the blanks (by selecting from the listed set of words) in the answer booklet for the following questions:

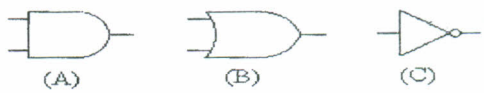
(NOT, OR, AND, NAND, NOR, XOR, XNOR, rise time, fall time, amplitude, transition time, period, pulse width, zero, infinite, positive-going edge, negative-going edge, Multiplexer, Demultiplexer, Encoder, Decoder, Comparator, Register, LOW, HIGH) (10 Marks; 0.5 Mark each)

S1. On a digital waveform, the transition time from a HIGH level to a LOW level is called _____.
S2. On a digital waveform, the interval between pulses is called _____.
S3. For an ideal digital pulse, transition times are _____.
S4. For a negative-logic pulse, the leading edge is the _____.

In the shown nonideal pulse:



S5. Item (1) represents _____.
S6. Item (2) represents _____.
S7. Item (3) represents _____.
S8. Item (4) represents _____.



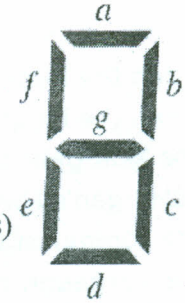
S9. The device in Fig. (A) is a(n) _____ function.
S10. The device in Fig. (B) is a(n) _____ function.
S11. The device in Fig. (C) is a(n) _____ function.
S12. The _____ circuit creates an output that indicates whether or not the input values are equal.
S13. The _____ circuit converts information into a specific coded form.
S14. The _____ circuit converts data from a serial to a parallel form.
S15. The _____ circuit is made up of flip-flops.
S16. In the 2-input _____ gate, a Low input gives a High output.
S17. In the 2-input _____ gate, a High input gives a Low output.
S18. In the 2-input _____ gate, a Low input gives a Low output.
S19. In the 2-input _____ gate, a High input gives a High output.
S20. In the NOT digital circuit, a _____ input gives a High output.

Answer the following regular questions in the answer booklet:

(2 questions - total of 35 Marks)

R1. For a two binary number multiplier (each consists of 2 bits): (15 Marks)
a- write the truth table of the multiplier. (4 Marks)
b- what is the optimized Boolean expresions for the first two least-significant-bits (LSBs) of the multiplier outputs. (6 Marks)
c- implement the logic circuits for the optimized expressions using only NAND gates. (5 Marks)

R2. For the 7-segment decoding logic, a BCD number is used as the input and the 7 outputs are used to activate the corresponding segments of the display. The arrangement of segments is as shown here: (total of 20 marks)



a- write down the truth table (use X to represent don't care output) for all 7 segments. (7 Marks)
b- develop the optimized Boolean logic expression of the **"e"** output segment. (8 marks)
c- develop the optimized logic circuit for segment "e". (5 marks)
Note: complements of inputs are available.