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University	: Menoufia		*Date*	: 29/12/2019
Faculty	: Electronic Engineering		*Time*	: 3 Hours
Department	: Comp. Science & Eng.		*No. of pages*	: 3
Academic level	: Prep. Year, 1st term		*Full Mark*	: 30 Marks of 60 Marks
Course Name	: Logic Design		*Exam*	: First term Final Exam
Course Code	: CSE 324		*Examiner*	: Dr. Ahmed Shehata Part II

إبدأ إجابة هذا الجزء من اليمين **(Part II)**

Answer the following questions

Question number 1: Select the best Answer [10 marks]

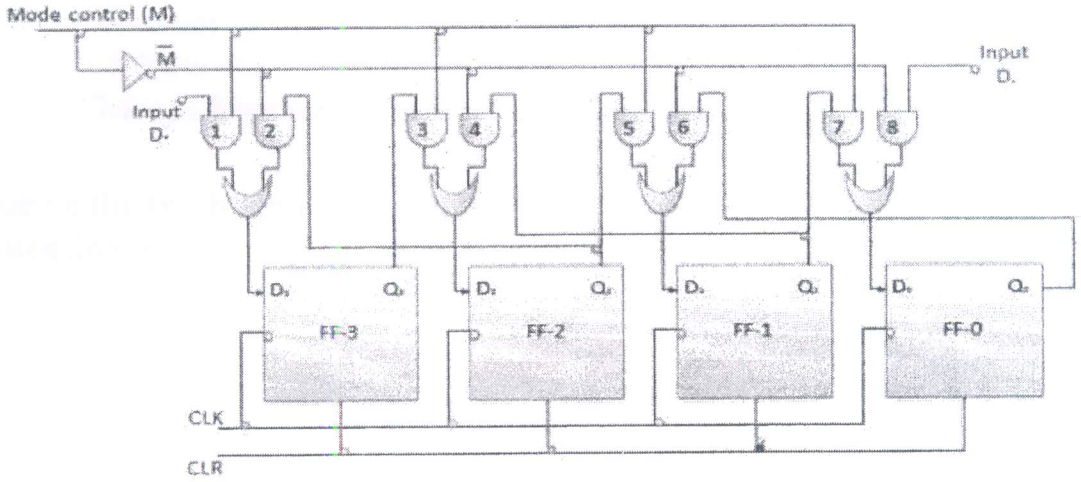
1. Decade counter counts from 0000 to _____ and back to 0000.
   A. 1001 B. 1111 C. 1000 D. 0000
2. In SR latch the R referred to _____
   A. Synchronous B. Reset C. set D. none
3. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay is _____
   a. 12 ms b. 24 ns c. 48 ns d. 60 ns
4. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____
   a. 0000 b. 1111 c. 0111 d. 1000
5. A type of shift register in which the Q or Q' output of one stage is not connected to the input of the next stage is _____.
   a. parallel in/serial out
   b. serial in/parallel out
   c. serial in/serial out
   d. parallel in/parallel out
6. A _____ is a circular shift register with only one flip flop being set at any particular time, all others are cleared.
   A. ring counter B. shift register
   C. binary counter D. none of these
7. How is a J-K flip-flop made to toggle?
   a. J = 0, K = 0 b. J = 1, K = 0
   c. J = 0, K = 1 d. J = 1, K = 1
8. The only difference between a combinational circuit and a flip-flop is that _____
   a) The flip-flop requires previous state
   b) The flip-flop requires next state
   c) The flip-flop requires a clock pulse
   d) The flip-flop depends on the past as well as present states

9. A modulus-10 counter must have _____
   a. 10 flip-flops b. 4 Flip-flops
   c. 2 flip-flops d. Synchronous clocking
10. A bidirectional 4-bit shift register is storing 1101. Its input is HIGH. The digits 1011 is waiting to be entered from first left FF on the serial data-input line. After three clock pulses, the shift register is storing _____
    a. 1101 b. 0111 c. 0001 d. 1110

Question number 2:

a. Design a 3-bit register with parallel load. The register has a mode signal M, when M=0 the register will store its information, M=1 the register will load data. (4 Marks)

b. According the following figure answer questions (6 Marks)



1- The name of this sequential circuit is _____
2- Mode control M=0, the operation will be _____
3- Mode control M=1, the operation will be _____
4- Redraw the circuit using a multiplexer.

Question number 3:

a. Design an asynchronous modulo 6 counter using JK flip flop. (4 Marks)

b. Design a D synchronous counter that has the following sequence: 2,5,6 and repeat. The undesired states must always go to 6 on the next clock pulse. (6 Marks)

With my best wishes
Dr. Ahmed Shehata

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نصف العام ٢٠١٩ الاعدادى

Menoufia University
Faculty of Electronic Engineering
Department of Computer Science & Eng.,
Preparatory year

Final 1st Term Exam
Logic design
Date: 29-12-2019
Time: 180 min

Part I

1-Answer the following questions:

1-Complete the missing parts

$(16)_{10}= (\ldots)_2=(\ldots)_8=(\ldots)_{16}$

$(54.16)_8=(\ldots\ldots\ldots)_{10}=(\ldots\ldots\ldots)_{16}$

$(11)_{10}=(\ldots\ldots\ldots)_{2421}=(\ldots\ldots\ldots)_{Ex\text{-}3}=(\ldots)_{gray}$

(10 degree)

2- (a) Perform the following operations in 2's complement system. Use 8 bit (including the sign bit) for each number.

- Add +18 to -25
- Subtract +25 from -18
- Subtract -25 from -18
- Subtract 17 from 25using normal subtraction, and 1's complement method

2-(b) Drive the truth table of the full adder, then obtain the equations of S and C after implementing K-Map, then draw the logic gate design of both S, and C.

(10 degree)

3 (a) Simplify the following expressions using both of Boolean algebra, and K-map, then draw its ouput.

$Y= C(A\oplus B)+(B\oplus C)+A+B+C$

(b)- For 8-to-3 line encoder, draw its I/O truth table, deduce its output equations, and Dtaw its circuit diagram.

(10 degree)

مع اطيب تمنياتى بالتوفيق