Mansoura University — Fourth Year Electronics
Faculty of Engineering — May 2013
Electronics&Comm. Dept. — Time: 3 hrs

Integrated Circuits Final Exam [Total : 100 marks]

Attempt All Questions

1-a) True Or False : each statement with T Or F.
- The width of MOS transistor increases,its gate capacitance will decreases.
- MOS transistor with high Vt has less power and switch slower.
- Virtex-5,one slice contains two LUTs.

b) Short Answers.
- Give three reasons,differences between dynamic and static CMOS inverters....
- System-on- Chip (SoC) has .....
- Give three reasons, benefit of scaling .....

c) Explain : - FPGA computer aided design (CAD). - Define features of synthesis tools. - Integrated Software Environment(ISE).

d) Discuss,can build a CMOS buffer /inverter, the pull-up network with NMOS and pull-down network with PMOS.

2-a) Implement the following functions using programmable logic array:

$$W = ABC + A\overline{B}C + \overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\overline{C}$$

$$X = \overline{A} + BC$$

Define the types of its outputs.

b) Explain CMOS transistor fabrication steps and define testing , packaging, and its problems.

c) Calculate the noise margins of the DMD, with the parameters:
$V_{DD} = 3.3$ V $V_{TD} = 0.6$ V $V_{TU} = -0.8$ V knu =knd = 60 μA/ V^2
(L/W)d =4 (L/W)u = 24

3-a) Prove that static CMOS inverter is ratioeless.
Define its properties and noise in digital ICs.

b) Design a CMOS inverter with the following paramters :
$V_{DD} = 3$ V $V_{TN} = 0.6$ V kn = 40 μA/ V^2
(W/L)p= 2.5 (W/L)n $V_{TP} = -0.8$ V kp = 16 μA/ V^2
Calculate the noise margin of the circuit.

4-a) Draw a pull down network shown in Fig. 1. Write the Boolean logic function. Sketch its stick diagram.

b) Explain why dynamic logic,and why not? . Discuss domino logic gates and its problems.

c) Implement 2-input NOR gate using BiCMOS technique. Explain such circuit is faster than static one.

5-a) Find the Wn/Wp ratio of a Pseudo NMOS inverter with the following parameters:
NMOS $V_{TN} = 0.6$ V kn = 60 μA/ V^2 Ln = 0.8 μm
PMOS $V_{TP} = -0.7$ V kp = 45 μA/ V^2 Lp = 0.8 μm
Assuming $V_{DD} = 3.0$ V , Vin = V_{DD} and $V_{OL} = 0.22$ V

b) What are the factors affected on a pseudo NMOS inverter ?

c) Implement $F = (X_1X_2 + X_3X_4)(X_5 + X_6)$ using NP CMOS ligic.
Let $F1 = (X_1X_2 + X_3X_4)$, $F2 = (X_5 + X_6)$,and F =F1 $\overline{F2}$

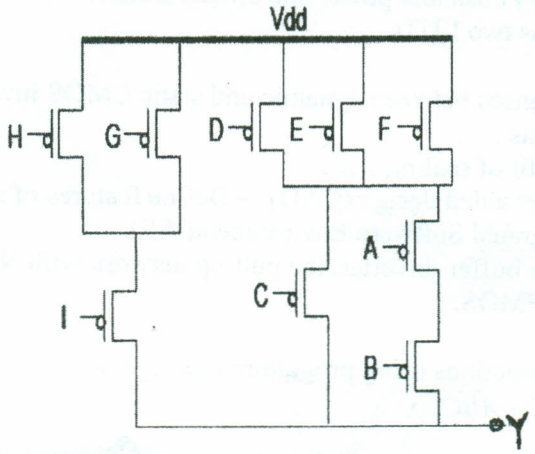

Fig. 1