FPGA Based Speed Control of Three-Phase Induction Motor Using Stator Voltage Regulator

استخدام ال FPGA للتحكم فى سرعة المحرك الحثى ثلاثى الطور باستخدام متحكم فى جهد العضو الثابت"

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الملخص : فى هذا البحث تم بناء طريقة رقمية ب استخدام الFPGA للتحكم فى سرعة المحرك الحثى ثلاثى الأطوار. هذه الطريقة تعتمد على تغيير الجهد الداخل للعضو الثابت الخاص بالمحرك للتحكم فى سرعته. و النظام المقترح يتكون من ستة مفاتيح. و الطريقة الرقمية المقترحة تستخدم موجة سن المنشار بتردد ضعف تردد المصدر كموجة تحكم ليتم مقارنتها بموجة مثلثية كموجة حاملة. و يمكن التحكم فى الجهد الخارج من من مقطع التيار المتردد عن طريق تغيير مستوى جهد موجة التحكم (سن المنشار). تقدم طريقة التحكم الرقمية أيضا نظام بدء جيد للمحرك الحثى ثلاثى الأطوار. و يتم عمل نظام البدء عن طريق جعل جهد موجة سن المنشار أقل ما يمكن و زيادتها تدريجيا خلال فترة البدء. تم استخدام برنامج PSIM لعمل المحاكاة الخاصة بهذا النظام. و تم استخدام الFPGA لبناء طريقة التحكم الرقمية. و تم تقديم التصميم الرقمى للنظام باستخدام FPGA بالتفصيل. تم مقارنة النتائج التى تم الحصول عليها من المحاكاة مع التى تم الحصول عليها من النموذج المعملى. أوضحت نتائج المحاكاة و النتائج المعملية تشغيل متزن خلال فترة التشغيل الطبيعية. مستوى التوافقيات فى تيار المصدر و تيار المحرك و معامل القدرة تم عرضها فى ظروف التشغيل المختلفة.

Abstract — In this paper a digital speed control strategy for three-phase induction motor is implemented. This strategy depends on varying the stator voltage to control the speed of induction motor. The system consists of six bidirectional switches. The digital control strategy uses saw-tooth waveform with twice the supply frequency as a control signal to be compared with triangular waveform as a carrier signal. The voltage output from ac voltage regulator can be controlled by varying the voltage level of saw-tooth waveform. The control strategy provides also soft starting for the induction motor. The soft starting is implemented by starting the motor in low value of modulation index and increasing it gradually during the starting period. The simulation of the system is carried out by PSIM computer program. The control strategy is implemented by using FPGA. A detailed digital design of control system has been introduced in details. The simulation results have been compared with the experimental results from laboratory prototype. The simulation and experimental results show stable operation for wide range of speed control. The levels of harmonics in the supply and motor currents and power factor have been evaluated for different operating conditions.

I. INTRODUCTION

The availability of microprocessors, microcontrollers, and digital signal processors (DSP) facilitates the digital implementation of control system of electrical machines. The DSP is the most commonly used device for such applications. The DSPs are highly optimized application-specific microprocessors designed to process signals, including control signals. With the increasing density and complexity of field programmable gate arrays (FPGAs), programmable architectures are becoming more attractive for implementing embedded system designs. FPGAs are increasingly coming into their own as a way to achieve application specific integrated circuits (ASIC) like performance-levels with hardware that has off-the-shelf convenience similar to traditional DSP processors. Sophisticated control algorithms become easier to be implemented with FPGAs. One of the fundamental advantage of FPGA over DSP or other microprocessors is the freedom of parallelism. Since different parts of FPGA can be configured to perform independent functions simultaneously, its performance is just not tied to clock rate as in DSPs. The FPGA provides a low cost control for induction motor by many control strategy [7].

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Three-phase ac chopper is one of the simplest ways to control the speed of induction motor. AC choppers have been used to control both static and dynamic loads [1-3]. Three-phase ac chopper has been used to feed three-phase induction motor [4,5]. Single-phase and three-phase ac choppers are showing cost reduction and effective control. The main problems associated with the ac choppers are the high harmonic contents in the supply and motor currents, very poor power factor especially at light loads, and low efficiency. Modern PWM techniques can help in modifying these performance parameters [1,6]. Using FPGA can generate the required PWM switching function easily and economically.

The essence of this paper is to explain the design of digital speed control strategy of three-phase ac chopper under three-phase induction motor load by using FPGA.

II. SYSTEM UNDER STUDY

The proposed system consists of six bidirectional switches as shown in Fig.1. Three switches are connected in series with stator terminals of the motor and another three are used to provide freewheeling path across stator windings. In this study a saw-tooth PWM strategy has been used to control the speed of three-phase induction motor. Saw-tooth PWM is characterized with high power factor, lower THD at machine currents and high frequency component of supply current which can be easily removed by using simple passive filter. Fig.2 shows the waveform of switching signal of series switch, motor voltage and its FFT components for saw-tooth PWM strategy.

III. MATHEMATICAL MODEL FOR SAW-TOOTH PWM CONTROL STRATEGY

The relation between motor phase voltage and supply voltage can be expressed as:

$$v_r(\omega t) = S_x(\omega t) * v_s(\omega t) \quad (1)$$

where, $S_x(\omega t)$ is the switching function and $v_r(\omega t)$, $v_s(\omega t)$ are the motor and supply voltages.

All the PWM schemes are designed with certain switching frequency f_s and the modulation frequency, m_f and the modulation index, m_a. The main function of the PWM is to produce near sine-wave supply current with very low amplitude high frequency harmonic contents. Simple filters can easily remove such low amplitude-high frequency harmonic contents. The main problem associated with PWM technique is the relatively high switching losses.

In saw-tooth PWM control strategy of a three-phase ac chopper, the switching function can be obtained by comparing negative slope saw-tooth signal with triangular signal as shown in Fig.2. The same switching function can be obtained in digital manner by using FPGA as shown in this study. The negative slope saw-tooth PWM, SPWM is introduced to improve the input power factor and THD of the three-phase ac voltage regulator. The saw-tooth waveform has its peak at the intersection of phase voltage with the time axis, i.e. the saw-tooth wave of which the frequency is twice as that of ac supply. The control has been done by adding or subtracting a dc component to the saw-tooth signal. So, the slope of the saw-tooth signal is always constant, but the amplitude is varied with. The modulation index, m_a is the ratio between the peak values of the saw-tooth to the peak of triangular signal as shown in (2).

$$m_a = \hat{V}_{Saw} / \hat{V}_{tri} \quad (2)$$

where: $\hat{V}_{Saw}$: peak value of the saw-tooth signal.

$\hat{V}_{tri}$: peak value of the triangular signal.

The output voltage is changing with the modulation index in the over-modulation region (m_a>1). In the linear region ($0 < m_a < 1$), the fundamental component of the motor voltage is directly proportional to the value of m_a as shown in (5). The continuous time varying of motor voltage can be obtained by using Fourier transform of switching function and using the results in (1). The continuous time varying of motor voltage of SPWM is:

$$v_r(\omega t) = \left(\frac{m_a}{2} + \frac{1}{4}\right) V_m \sin(\omega t) + \frac{V_m}{4\pi} \sum_{n=1}^{\infty} \left[\frac{1}{n} \cos(n\omega t)\right] \quad (3)$$

The continuous time varying fundamental component of motor voltage of SPWM is:

$$v_{r1}(\omega t)=\frac{V_m}{4\pi}[\pi(2m_a+1)\sin(\omega t)+\cos(\omega t)]; \quad (4)$$

Then, the rms of fundamental component of motor voltage is:

$$V_{r1}(\omega t)=\frac{V_m}{4\sqrt{2}\pi}\sqrt{\pi^2(2m_a+1)^2+1} \quad (5)$$

The angle of V_{r1} with respect to supply voltage is Ψ_1 where;

$$\Psi_1=\tan^{-1}[1/[\pi(2m_a+1)]] \quad (6)$$

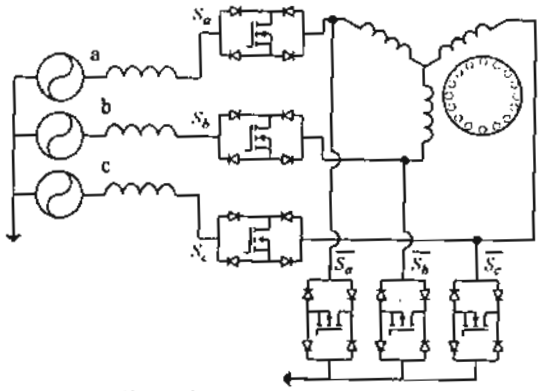

Fig.1. System under study.

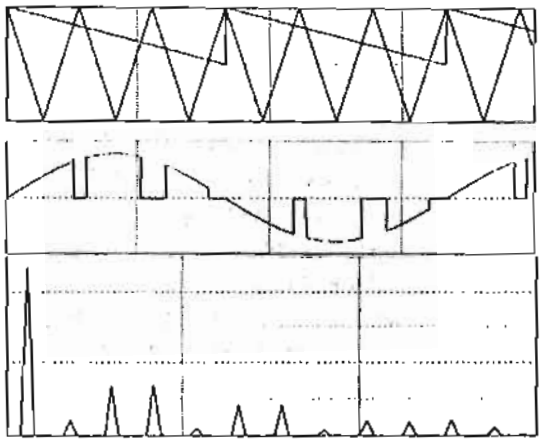

Fig.2. Saw-tooth, triangle, motor voltage waveforms and FFT components of motor voltage.

IV. DIGITAL IMPLEMENTATION OF SPWM

The digital control system for the laboratory prototype was implemented using Spartan3E starter kit. This kit incorporates XC3S500E FPGA from Xilinx and a lot of other peripherals to make the development of digital control and embedded systems such an easy task. The package used is fg320 with speed grade of -4 and 500k system gates. Xilinx ISE 9.1i Web-Pack edition with VHDL are used as developing environment and programming language.

The block diagram of the digital control system is shown in Fig.3. This system uses three saw-tooth generators each of them is synchronized with one of the supply voltages. The synchronization is achieved by detecting the zero crossing point of phase *a* voltage (only negative to positive transitions are detected). Another module of this system is dedicated to control the modulation index. This module shifts each saw-tooth up or down to change the modulation index in the range from 0 to 1.5. A triangular generator is used to generate a triangular waveform with a frequency of 360Hz (as an example to make the frequency modulation equal to 360/60=6 and it is easy to change this value). The triangular waveform oscillates between zero-voltage to the peak-voltage. This means that the triangular and saw-tooth waveforms are shifted up by the value of the peak to avoid representing negative values in FPGA. Each saw-tooth is compared with the triangular signal (after adding the shift value). Comparators outputs and their negations are passed to dead beat time module then to the output buffers. The control system is divided into seven modules as shown in the following sections.

A. Triangular Generator

The triangular generator was implemented in FPGA like an up-down counter where a clock input is fed to a counter, *m*. This counter resets to its maximum value *m* each time phase *a* voltage cross its zero level (negative to positive crossings only). The counter counts from its maximum value down to 0 then counts in the opposite direction from 0 to *m* and so on. So the triangular generator counts a total number of 2*m* counts in each cycle of switching period. The clock used to trigger the counter has a frequency of 50MHz, so the frequency of the generated triangular waveform f_s can be calculated from the following relation:

$$f_s = \left(50\times10^6\right)/2m \quad (7)$$

f_s equals 360Hz (as an example), so m can be calculate from the above equation as following:

$$m = \frac{50\times10^6}{2\times f_s} = \frac{50\times10^6}{2\times360} \approx 69444 \quad (8)$$

B. Saw-tooth Generator

Each saw-tooth generator is implemented like a down counter. Each counter counts from $m/2$ down to 0. Every counter is synchronized with one phase of the three phase line voltages; each of them starts counting from its maximum value with the zero crossing of the appropriate phase (negative to positive crossings only). The counters recycle when the value of minimum counts is reached. The saw-tooth waveform has to oscillate at a frequency $2f_1 = 120Hz$, so the counters should be triggered using a clock frequency f_c calculated by the following relation:

$$f_c = \left(f_s \times m\right)/2 = \left(120\times69444\right)/2 = 4166640Hz \quad (9)$$

So, f_c can be generated by dividing the main system frequency (50MHz oscillator exists on the board) by 12 as shown in Fig.5.

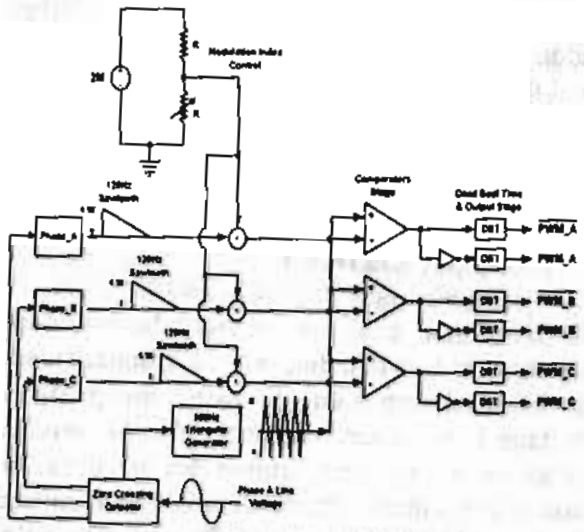

Fig.3. The block diagram of the digital control sysem.

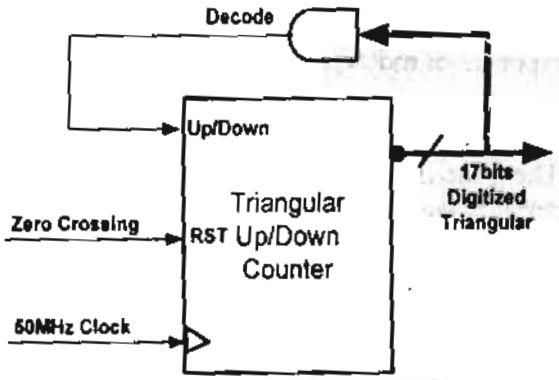

Fig.4. The schematics of triangular generator module.

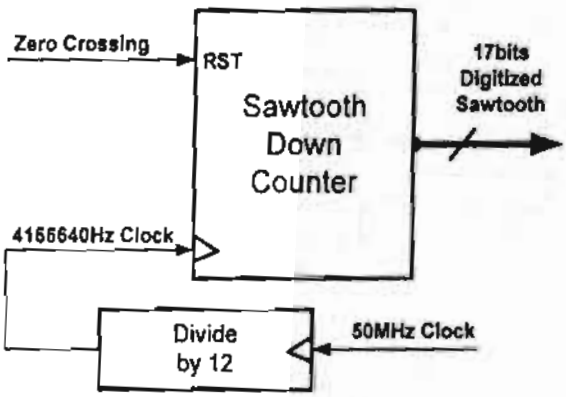

Fig.5. The block diagram of saw-tooth generator.

C. Zero-Crossing Detectors

A simple analog comparator used to compare phase a voltage with zero level. The comparator produces square wave voltage which is sampled by FPGA to determine the instant when the square wave goes from low to high (zero crossing) by using zero-crossing module. The block diagram of zero crossing circuit is shown in Fig.6. The generated pulse can be directly applied to the three saw-tooth generators where each generator resets to a value corresponding to the phase delay for each phase. Phase a saw-tooth will reset to its maximum value $m/2$ which corresponds to a zero phase delay. Phase b saw-tooth will reset to $m/3$, and phase c saw-tooth will reset to $m/6$ as shown in Fig.7.

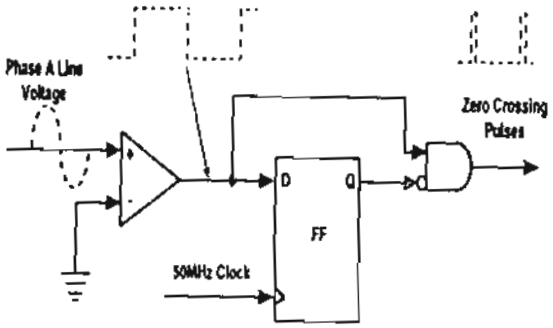

Fig.6. The block diagram of zero-crossing detector circuit.

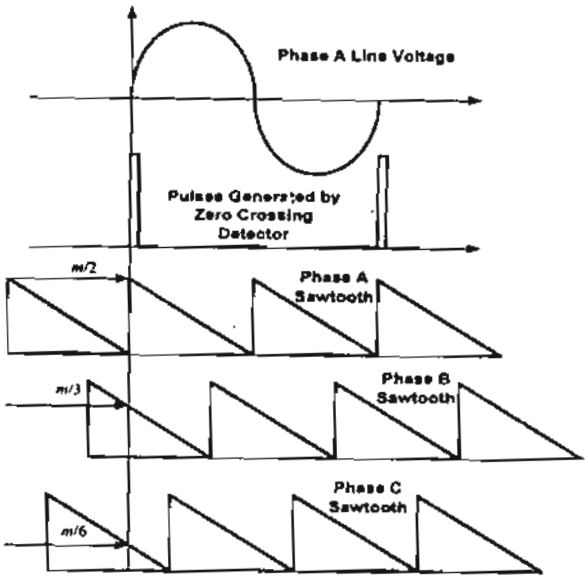

Fig.7. The timing for zero-crossing detector.

D. Modulation Index Control

The starting value of the modulation index is set to zero to reduce the output voltage to starting the motor at low voltage to avoid high starting current. By adding a variable value from 0 to m into the generated saw-tooth, the value of the modulation index varies from 0 to 1.5. A simple increment/decrement module was used to generate this adjustable value. The value of this variable can be adjusted using two push buttons on the FPGA. A block diagram of this module is shown in Fig.8. The output is incremented/ decremented by a fixed step every 0.1 second so the system clock was divided by $5*10^6$ before being applied to this module. A reset signal is used to force the modulation index to be 0 at any time. The output of this module can be added to the output of saw-tooth generators before comparing with triangular waveform.

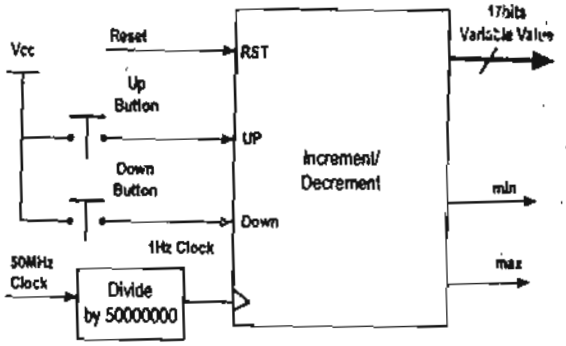

Fig.8. The modulation Index control module.

E. Digital Comparators

Saw-tooth waveform is added to the modulation index variable and then compared with triangular generator using a digital (binary) comparator. The binary comparator outputs logic '1' if the value of saw-tooth wave less than the value of triangular; otherwise it outputs logic '0'. A reset signal can force the comparators outputs to logic '0' at anytime. Each of the comparator outputs is negated to produce the complement signal of each value. Comparator output is used to trigger the shunt switch in power circuit, while its complement used to trigger the series switch in the same phase circuit. The block diagram of digital comparator module is shown in Fig.9.

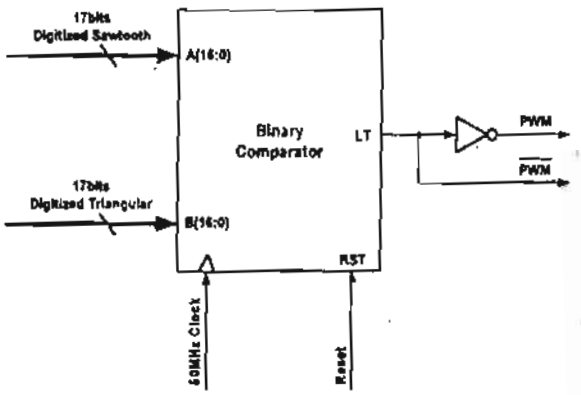

Fig. 9. The block diagram of digital comparator module.

F. Deadbeat Time

It is required to provide a dead beat time in each transition between any series and shunt switches to avoid sudden short circuits or voltage and current spikes. The deadbeat time insertion was embedded after the outputs of the comparators. Every comparator output and its complement are subject to an adjustable delay

when they switch from logic '0' to logic '1'. The deadbeat time can be adjusted using two push buttons, these push buttons control the frequency of the clock which is used to trigger deadbeat time delay registers. The control over deadbeat time is achieved by controlling the divider value which is used to divide the main system clock (50MHz). The time value of the deadbeat time is shown on the monitor of FPGA. The block diagram of deadbeat time module is shown in Fig.10.

An inverter placed at each output to counteract the negation done by using the optocoupler used between the control and power circuits.

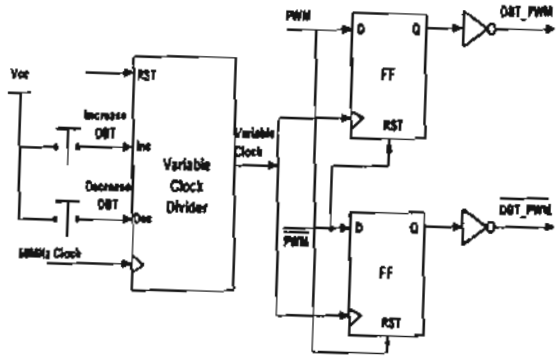

Fig.10. The block diagram of deadbeat time module.

G. LCD Controller

As a part of system design; it is required to display the modulation index and deadbeat time values on a LCD screen. The development kit incorporate LCD module which can be used to show any data. The LCD is 2 lines, each line consists of 16 characters. PicoBlaze is a soft 8 bits microcontroller provided by Xilinx as a royalty free IP. This microcontroller is used to control the LCD module. For simplicity; a counter is used to hold the number of times the user press modulation index push buttons (up/down buttons), then a look up table (LUT) is used to convert these counts directly into the modulation index value. The range from 0 to 1.5 of modulation index is divided into 256 steps, and each step corresponds to about (0.006) increase/decrease in the modulation index value. Pre-calculated modulation index values were stored in the LUT and the number of steps was used to access the LUT and produce 20bits of 5 digits BCD representation of the current modulation index value. Then PicoBlaze reads these digits, converts them to ASCII codes, and sent them to LCD module using the appropriate method (refer to Spartan3E starter kit data sheet for more information). The same technique was used to display the deadbeat time value on the LCD. Fig.11 shows a simplified block diagram of the LCD controller.

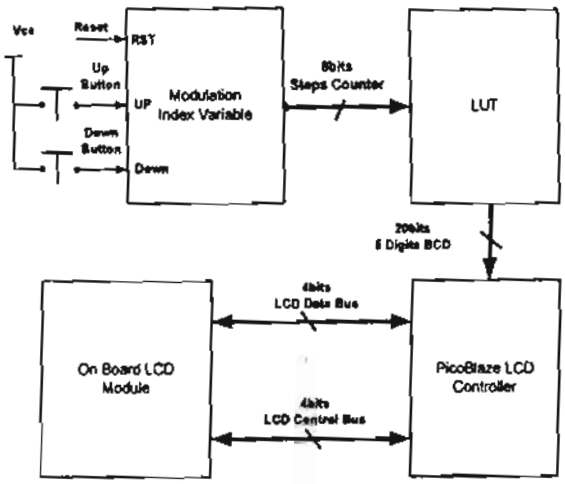

Fig. 11. The block diagram of LCD controller module.

V. SIMULATION AND EXPERIMENTAL RESULTS

The simulation of the ac voltage regulator for different strategies has been carried out by using PSIM computer program [8]. The induction motor used in the study is a 380V, 3.81 A, 1.0 kW, 60 Hz and 4 poles. Its parameters are shown in Table(1).

Table (1) The induction motor parameters.

R_s, Ω	R_r, Ω	$L_s = L_r$ H	L_m H	N, rpm
3.13	1.74	0.008334	0.1369	1770

The power circuit consists of the following:

1- The power MOSFET n-channel (Part # IRFPC50) has a V_{DSS}=600V and Id=11A

2- The ultra-fast recovery diodes used in bidirectional switch is (#RURP860) has a high-reverse voltage (600 V), low-forward voltage drop (1.5 V at 8 A),

3- Snubber circuit to protect the power MOSFET.

4- Three-phase supply and induction motor.

Fig.12 shows the experimental result of supply current with respect to phase a voltage. Fig.13 shows the variation of THD of supply and motor currents with motor speed at rated load. It is clear from this Fig.that the THD of supply currents contains high harmonics level. The harmonic components in supply current have a frequency around switching frequency, so it is easy to remove it by using simple passive filter. Fig.14 shows the power factor with motor speed at rated load.

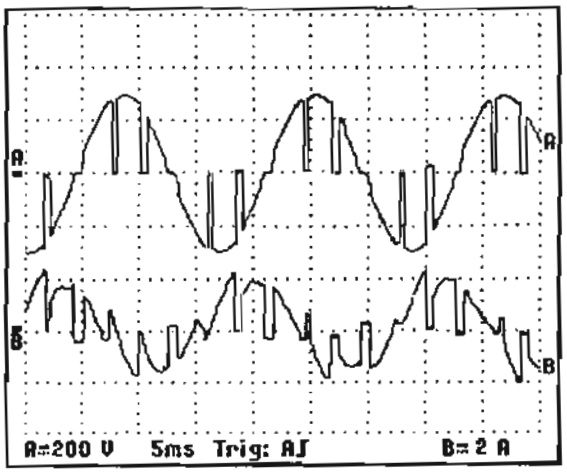

Fig. 12. The experimental result of supply current with respect to phase *a* voltage.

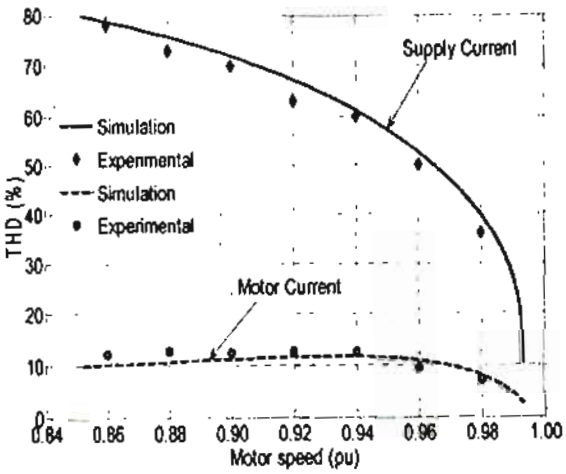

Fig. 13. The variation of THD of supply and motor currents with motor speed.

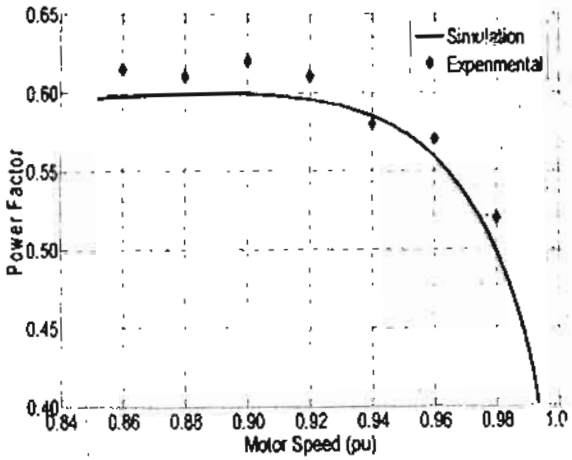

Fig. 14. The variation of power factor with motor speed.

VI. CONCLUSIONS

Three-phase ac choppers provide a simple and low cost option for speed control of three-phase induction motor. Invention of modern fast switches as IGBT and MOSFET improves the performance of ac voltage regulators. Saw-tooth PWM control strategy is used for speed control of thee-phase induction motors to improve the motor performance. FPGA is used in producing the required switching signal in efficient manner. The FPGA provides a digital control for the induction motor. The digital control system provides a speed control and soft starting technique for the induction motor. The digital control system provides on line controllable deadbeat time. The modulation index and deadbeat time are shown on the built in LCD screen.

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