University	:	*Menoufia*		*Date*	: *10/1/2019*
Faculty	:	*Electronic Engineering*		*Time*	: *3 Hours*
Department	:	Computer Science and Eng.		*No. of pages*	: *2*
Academic level	:	*3th Year*		*Full Mark*	: *70 Marks*
Course Name	:	Computer architecture		*Exam*	: *Final exame*
Course Code	:	CSE 361		*Examiner*	: *Dr. Mervat Mousa*

Answer all the following questions

Question NO 1 (11 marks)

a)Define

1)Structure 2) function

b)Draw with definition every level of transformation for an electronic computer system

c)Draw and describe Von Neumann Architecture

Question NO 2 (13 marks)

a)If you give a word-addressable main memory consisting of four blocks, and a cache with two blocks, where each block is 4 words. What is address bit of a cache and and How can store the content of address 13 in the cache memory ?

b)What is meant by I/O protocol ?

c Draw and explain the sharded input -output structure to concept the I/O protocol, what is the advantage and disadvantage of this structure.

d) Draw and explain the Static Random Access Memory (SRAM) and how to write operation 1 and 0

Question NO 3 (19 marks)

a) complete the words in the following sentence

1) The storage element for a static RAM is the _____.

2) EPROMs can be erased by_____

3) Dynamic memory cells store a data bit in a _____.

4)Type of ROM can be erased by an electrical signal named _____

5) An _____contains machine language instructions, but it does not contain code for any library routines that may be necessary

b) How many address lines would be required for a 2K × 4 byte memory chip ?

c)A computer has a five-stage instruction pipeline of one cycle each as shown in the following figure The five stages are: Instruction Memory (IM), register file (Reg), instruction execution in (ALL) , read or write data in (DM). write back data in (REG))

1) Draw the pipeline structure and explain the hazards in the following code

```
SUB  $2,  $1,  $3
OR   $12, $2,  $5
SW   $13, 100($2)
ADD  $14, $2,  $2
LW   $15, 100($2)
```

2)How can solved the above code without hazard ?

d) Processor has a direct mapped cache - Data words are 8 bits long (i.e. 1 byte), - Data addresses are to the word -A physical address is 20 bits long- The tag is 11 bits- Each block holds 16 bytes of data

1)what is the index and offset bit ? .2)- draw the address bit of the cache.

Question NO 4 (9 marks)

a)What is meant by Polling

b)Draw the register file and show by design internal architecture how to get an parallel 32 bit in the read line if the input register contains word of 32 bit

Question NO 5 (18 marks)

a)What is meant by path length

b) Draw the single cycle processor design of MIPS and show the contain of the hardware in the following

Instruction	RegDst	ALUSrc	Mem toReg	Reg Write	Mem Read	Mem Write	Branch	ALUOp 1	ALUOp 2	JMPReg
R- type										
Lw										
SW										
beq										
Jr										

c) Suppose we have a 32-bit MIPS word containing the value 0x008A1021. We would like to know what MIPS machine instruction this represents.

1)Write this instruction word in binary

2)What is the format of R instruction?

d)Convert the following equation to MIPS assamply

$x = (1 + y*y) / 2$

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